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Improvement of Cell Stability at Low Voltage Operation on 6T-SRAM Cell with 0.1μm Channel Width

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Abstract

Cell stability at low voltage operation has been investigated with fully manufactured 0.1μm channel width 6T-SRAM cell. Increasing the channel width ratio of driver to access transistor, which is typical method to enhance the static noise margin (SNM), is no longer effective in sub-0.1μm regime, because low voltage SNM is deteriorated due to inverse narrow width effect (INWE). To overcome the effect, the higher threshold voltages of cell nMOSFETs (driver and access) were effective for SNM improvement, but its method was limited by read current reduction, combined with narrow sensing margin. With separated Vth adjustment process, cell stability was improved by recovered SNM as well as read current.

1. Introduction

Scaled-down SRAM cells associated with low operation voltage has been emphasized, since low power dissipation and high reliability against hot carrier degradation are the major concerns of customers. However, the static noise margin (SNM) of the cell was degraded as the operation voltage decrease, because cell mismatches and soft errors were not scaled down with supply voltage. Hence it is getting harder to design SRAM cell with sufficient noise margin in low voltage operation regime.

SNM of SRAM cell mainly depends on the ratio of the transconductance of the driver and access transistors ($r= \beta_{DRIVER} / \beta_{ACCESS}$) referred to cell ratio [1]. In spite of area penalty, it has been inevitable to design larger channel width of driver transistor than that of access transistor to enhance SNM by achieving large cell ratio. However, for nMOSFETs with shallow trench isolation structure, threshold voltage decreases with shrinkage of device width, and this inverse narrow width effect (INWE) should be considered in designing SRAM cell under sub-0.1μm regime. In this paper, cell instability at low voltage operation has been analyzed with different cell ratio and threshold voltage variation, combined with peripheral transistor performance.

2. Device Fabrication

6T SRAM Cells were fabricated using p-type(100) Si wafer. Shallow trench isolation (STI) of 0.3μm depth was performed to realize the 0.1μm channel width. Gate oxide of nominal thickness of 35Å was used, and poly-Si/W silicide stack single gate layer deoposited. Gate length was 0.1μm. After S/D foramaton, the inter-layer dielectirc (ILD) oxide by PECVD was deposited over the wafer and the 0.1μm diameter of borderless contact was performed by PR flow method in photolithography. After W-plug formation, W-damascened local interconnection and metal line as a bit-line were fabricated to complete the memory cell. The top view of SEM image of 6-transistor of SRAM cell layout and critical dimension of driver and access transistor were presented in Fig. 1.

3. Results and Disscusions

Static Noise Margin shows cell's ability to retain its data state and the worst situation for retaining its data state is under "read-disturb" condition [2]. That is, when the access transistor turns on and connects the pre-charged bit-line to the low side of the cell, data state might be flipped if the voltage of low node is raised to a high level enough to reduce the voltage difference. Table 1 shows the result of 'read-disturb test' of which purpose is to check the weak cell, which data state flips during the test. Fail bits were observed with lower threshold voltage group under hot temperature test condition. In the previous study [3], the threshold voltage mismatch is aggravated at elevated temperature, and SNM is considerably sensitive to the operating temperature. Disappearance of data flip fail with high threshold voltage group is easily explained with Fig. 2, which were the simulated voltage transfer curves of cell.

Cumulative fail bits as a function of operation voltage is shown in Fig. 3. As operation voltage was decreased, fail bits were increased, and it showed higher failure rate at cold temperature test condition. According to the simulation result in Fig. 4, developed voltage (ΔV) and developed time (Δt) at cold temperature became too small to detect the signal on sense-amplifier operation. Furthermore, drain current of peripheral transistor was increased as much as the mobility enhancement at low temperature, contrast to constant saturation current behavior of cell transistor (Fig. 5). The discrepancy between peripheral and cell transistors performance at cold temperature were the main cause of higher bit failure rate on SRAM cell.

Even channel width ratio of driver and access transistors were increased to enhance the cell ratio, the measured threshold voltage and drain current at low voltage region was reversed due to INWE, shown in Fig. 6 and resulted in weak SNM characteristics (Fig. 7). Vth was inversely proportional to the channel width (Fig. 8), and it has been reported that narrow width effects is nearly a linear dependence on the potential rise at the edge of the channel width [4]. Atsuki, *et al.* observed that INWE is strongly related to the decrease of boron concentration near isolation edge [5].

As mentioned above, the high Vth and channel width increase of transistor didn't provide complete noise margin window due to the reduction of read current and INWE in given process condition, respectively. Fig.9 shows SNM and read current comparison between conventional and seperated Vth process. With optimization of Vth of each cell transistor separately, which compensated threshold voltage lowering of access transistor by additional implantation, read current is enhanced to the extent of 70% of initial current under the same value of SNM. This process was enable to widen the process integration window and was a method to extend to deep sub-micron device with sufficient SNM characteristics.

4. Summary

Increasing the channel width ratio of driver to access transistor was not effective in sub-0.1μm channel width regime, since it leaded to deterioration of the low voltage SNM by INWE. With the elevation of threshold voltage of cell nMOSFETs, SNM was improved but cell current reduction exceeded the permitted limits to cell operation. With seperated Vth adjustment process, both of SNM and cell current were obtained to the extent of acceptable level for mass production. The seperated cell Vth scheme provides sufficient SNM characteristics on SRAM cell with 0.1μm channel width and the beyond

References

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[2] Terence B. Hook, IEEE Trans, Electron Device (2002)1449
[3] Oleg Semenov, IRW Final Report (2002) 168.
[4] Kelvin Kuey-lung, IEEE Trans, Electron Device (1988) 325
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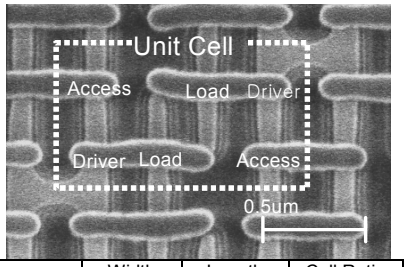

	Width	Length	Cell Ratio
Driver	105nm	100nm	1.1
Access	100nm	105nm	

Fig.1 Top view SEM image of SRAM cell after gate patternning: The unit cell area is 0.84μm^2.

VCC	Vth of driver ~0.65V		Vth of driver ~0.8V	
	-20℃	85℃	-20℃	85℃
0.5V	79	113063	3	34820
0.6V	22	271	1	27
0.7V	0	0	0	0
0.8V	0	0	0	0
0.9V	0	0	0	0
1.0V	0	**12**	0	0
1.1V	0	**29**	0	0
1.2V	0	**27**	0	0
1.3V	0	**13**	0	0
1.4V	0	**1**	0	0
1.5V	0	0	0	0
1.6V	0	0	0	0

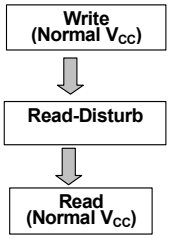

Table 1 Test result of 'read-disturb test' with temperature and Vth variation; Fail bits were observed on lower Vth group under hot temperature ambient test.

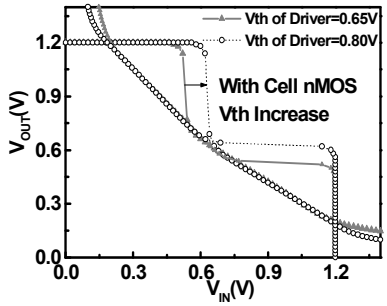

Fig.2 SPICE-simulated low voltage butterfly curves with variation of Vth of cell nMOSFETs.

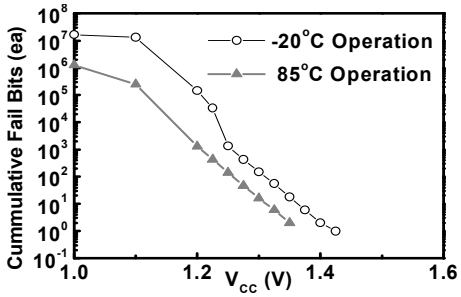

Fig.3 Cumulative fail bits as a function of operation voltage.

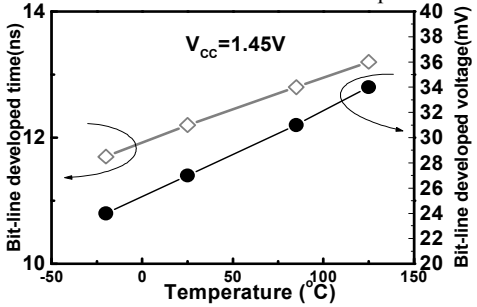

Fig.4 Temperature dependence of simulated bit-line developed voltage (ΔV) and developed time (Δt).

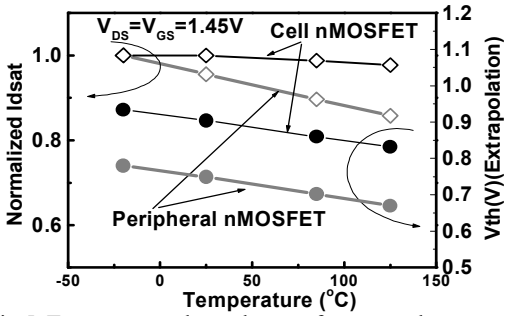

Fig.5 Temperature dependence of measured saturated drain current and threshold voltage.

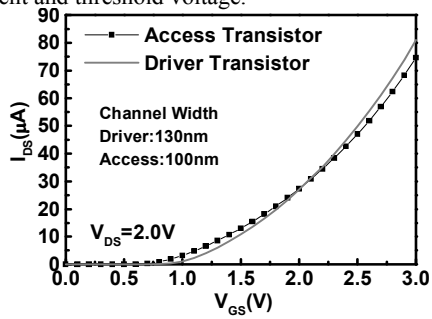

Fig.6 Measured Ids-Vgs curves for drive and access transistor with large channel width ratio group.

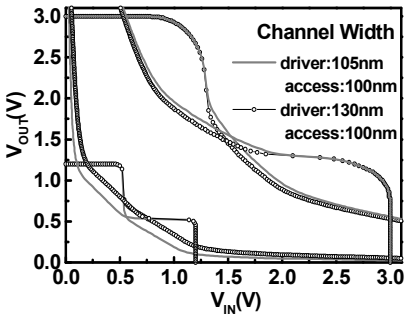

Fig.7 Meausered butterfly curves for two types of cells. High V_{CC} SNM improved but low V_{CC} SNM degraded for large channel width ratio group.

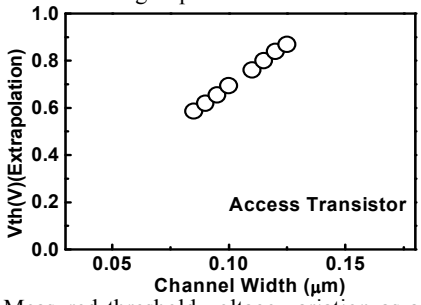

Fig.8 Measured threshold voltage variation as a function of channel width of access transistor.

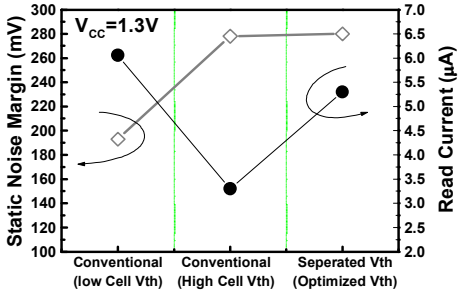

Fig.9 SNM and read current comparisons between conventional and seperated Vth process.