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Abnormal Disturb Mechanism of sub 100nm NAND Flash

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Abstract

The abnormal program disturb mode was found in NAND flash memory which was fabricated with 0.09-um CMOS STI process technology. This abnormal disturb mainly occurs in cells next to source select line (SSL) transistor and is not suppressed even if program bias is not applied. This unexpected program disturb is hot carrier program which results from high electric field between SSL transistor and its nearest cell and leakage current to boosted channel.

Keywords: NAND, flash, disturb, hot carrier, program

Introduction

The program disturb of a NAND cell is shown in Fig. 1. The Vpass disturb happens to the unselected cells in series with the "0"-program cell. On the other hand, the program inhibit bit line is applied to Vcc. The cells in inhibit bit line and same wordline with "0"-program cell is subjected to the Vpgm disturb[1]. But as cell size decreased under 100nm scale, an abnormal program disturb mode was found. Most of this program disturb occurs in cells next to source select line (SSL) transistor – cells in wordline 0. We will discuss this abnormal program disturb mechanism in detail, and suggest a brief model.

Experimental Results and Discussion

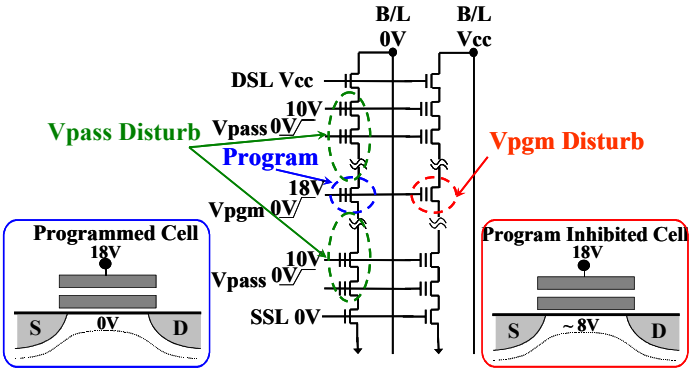

Fig. 1 Program disturb of a NAND-type cell

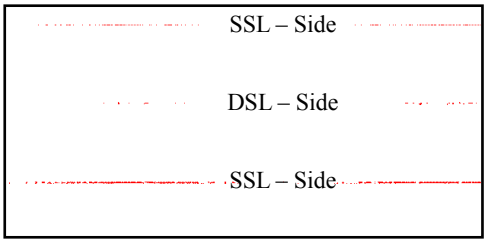

Fig. 2 Fail bit map of Vpgm disturb with 32 NOP test

Fig 2. shows Vpgm disturb fail bit map with 32 NOP (number of program pulse) test. Page addresses of all fail bits are 0/1(wordline 0, cell next to SSL) and 62/63(wordline 31, cells next to DSL-drain select line). Portion of 0/1 page is over 98%. The number of these fail bits at hot temperature are much more than at room temperature. Fig. 3 shows Vpass bias dependence of Vpgm disturb, where cells in wordline 0 and 31 have quite different behavior from cells in other wordlines. Unlike cells in wordline 1~30, disturbed Vt of cells in wordline 0 and 31 (especially wordline 0) increased with Vpass. Even if Vpgm bias is not applied, that is not suppressed. In normal Vpgm disturb mode, because the higher Vpass bias results in the higher boosted channel bias, Vpgm disturb can be reduced by increasing Vpass bias. If there exists channel leakage to silicon substrate, boosted channel bias drops. Then program disturb characteristics of all cells becomes worse. Because the difference of boosted channel bias & Vpass bias is small, program by F-N tunneling is impossible. These facts indicate that there exists another program disturb mechanism besides Vpass & Vpgm disturb, which is called boosted channel disturb(BCD). At hot temperature this BCD is worse than at room temperature (Fig. 3). Another possible program mechanism is hot electron program, which needs high electric field and current source into high field region. Because boosted channel bias is so high and channel bias of SSL transistor is fixed by SSL gate bias, there exists a high lateral electric field between SSL transistor and cell in wordline 0.

In order to find possible current source to high lateral field region, if exists, we tested cell junction leakage current and break down voltage at gated diode pattern which has real gate length(90nm) and real gate space(90nm). As shown in Fig. 4, junction break down voltage is about 9.8V and is

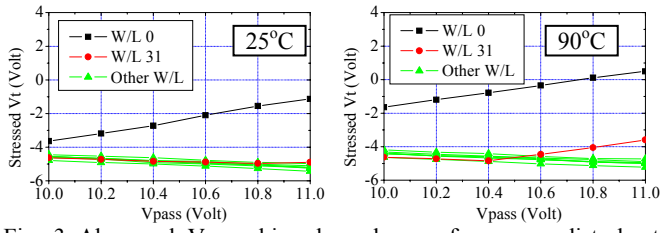

Fig. 3 Abnormal Vpass bias dependency of program disturb at different temperature (NOP 32)

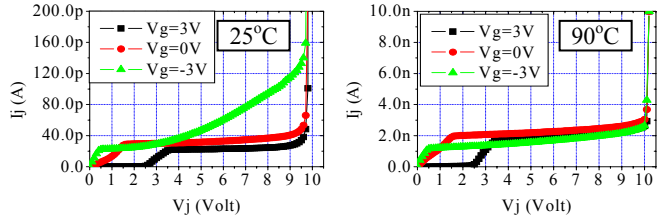

Fig. 4 Junction current vs. junction bias with various gate bias.

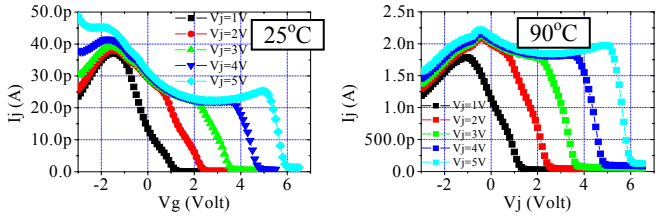

Fig. 5 Junction current vs. gate bias with various junction bias

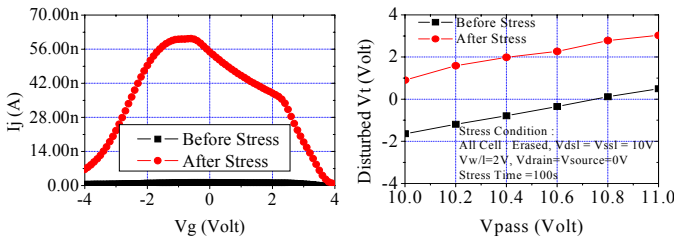

Fig. 6 Gate bias dependent junction current and BCD with fresh and degraded gate oxide at 90°C (DSL, SSL gate at BCD case)

almost independent of gate bias in range of -3 to 3V. Because used Vpass bias range is 10~11V, channel boosting level cannot exceed 9.8V. Therefore, this BCD is not related to junction break down. At room temperature, junction leakage current shows abrupt increase at junction bias around applied gate bias and then slowly increases up to break down voltage when positive gate bias is applied. At room temperature, -3V gate bias results in second steep increase with junction bias unlike positive gate bias case. At hot temperature, leakage current has almost same junction bias dependency in all gate bias conditions and the magnitude of current is about 50 times lager than at room temperature case. Even if Vg=-3V, we cannot see the second steep increase at hot temperature. One possible factor of slowly increasing current is that reverse bias current should depend on the magnitude of the reverse bias through depletion width. In order to clarify these junction current characteristics, we also measured gate bias dependence of junction leakage which is simple method to extract interface state (recombination-generation centers) at the oxide-silicon interface[2]. This indicates that first steep increase of Vj-Ij curve is generation current from oxide-silicon interface. As we can see in Fig. 5, gate induced drain leakage (GIDL) exists under about Vg=-1V. When Vg=-3V, second steep increase of Vj-Ij curve occurs due to GIDL. But around Vg=0V, GIDL seems to be negligible. Because GIDL is almost independent of temperature and generation current is strongly dependent on temperature, there is no explicit GIDL at hot temperature. Therefore, taking BCD temperature effect into account, we can infer that current source of hot carrier program is not GIDL but generation current due to interface state of oxide-silicon interface.

In order to confirm that current source of hot carrier program is the generation current at the oxide-silicon interface, we have measured BCD at cell array with degraded SSL & DSL gate oxide. The BCD test results and generation current at the oxide-silicon interface are shown in Fig 6. (Degradation method of SSL & DSL gate is described in inset of Fig. 6.) Stressed pattern has about 50 times lager interface generation current than fresh one, where we cannot see GIDL current as is the case of fresh pattern test at hot temperature. After stress, disturbed Vt of cells in wordline 0 and 32 increased significantly compared to that of fresh one. This shows the generation current at Si-Oxide interface is the

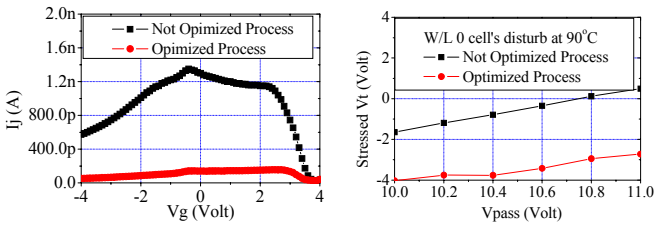

Fig. 7 Gate bias dependent junction current and BCD at optimized and not optimized technology at 90°C

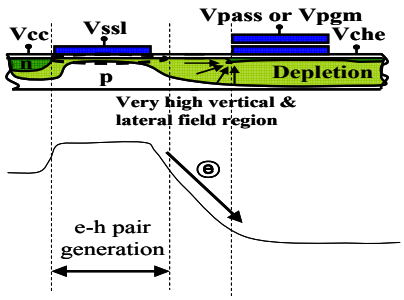

Fig. 8 Brief description of BCD

source of hot electron program. We can reduce this generation current about 1/10 by process optimization. Although it had relatively low junction break down voltage of about 9.4V, BCD at optimized technology is much suppressed as shown in Fig. 7. Therefore we can conclude that BCD is hot carrier program due to highly boosted channel bias and generation current from interface states between silicon and oxide.

Mechanism

Because of SSL transistor's gate bias condition, SSL transistor's channel region is completely depleted. Electron-hole pairs are generated from silicon and oxide interface of SSL transistor. Holes move to silicon substrate and electrons to cell region. Inverted channel of cells in wordline 0 takes most of electrons from junction between cell and SSL transistor. Therefore, junction becomes depleted. Highly boosted channel and short space between SSL and cells makes a high lateral electric field. Electrons that travel high field region became hot electron. These hot electrons can be injected to cells in wordline 0 through scattering(Fig. 8).

Conclusion

The abnormal program disturb is hot carrier program by high lateral electric field from SSL transistor to its nearest cells and by generation current due to interface state at the oxide-silicon of SSL and DSL transistor. As NAND flash cell size decreases, coupling of cells increases and the space from SSL transistor to cell decreases. Moreover, portion of gate edge to cell's total channel area increases. These facts suggest that scaling of flash memory cell makes this program disturb mode more serious.

References

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