Thorough Diagnoses of the Impact of Flash Memory Cell UV-State Threshold Voltage on the Cell Reliability and Program/Erase Cycling Endurance Performance

Victor Chao-Wei Kuo, Hann-Ping Hwang, Cheng-Tung Huang*, Cih-Wen Chou*, Shyang-Ming Tzeng, Chia-Ping Lai, Tzeng- Wen Tzeng, Yih-En Huang, Wei-Zhe Wong, Ching-Sung Yang and Saysamone Pittikoun;

E-mail: victor@psc.com.tw *: not with PSC anymore

TD2, Device Department, Powerchip Semiconductor Corp., Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C.

Abstract

In this paper, influences of the flash memory UVstate threshold voltage on the tunneling oxide reliability and the cycling performance have been discussed and clarified for the first time. By the result, high reliable flash with traditional stacked-cell is realized by utilizing the optimized UV-Vt technique. In our product, more than ten times longer enduring time is achieved by this method. In addition, exact solutions of nonlinear kinetics of the oxide N_{IT} degradation were clarified by DCIV test method for the first time, which also give the best explanations of the underlying oxide degradation mechanism during FN stress and flash cell operation.

Introduction

The operation of flash cell involves the high tunneling current flows through the oxide, which causes oxide-trapped charge (Not) and interface trap charge (Nit) to degrade the reliability of oxide. Hence, many experimental theses have been proposed to enhance the oxide reliability such as post oxidation annealing in nitrogen ambient. But oxide robustness the enhancement alone is not a faultless method to get a high enduring cell. The best way of promoting the reliability is to optimize the basic cell operation and the manufacturing process. Here, we discuss the most critical factor of the memory cell, UV-state Vt, which is closely related to the promotion of cell cycling performance.

Experiment

As shown in Fig. 1, there are two test devices utilized, one is dummy cell with a short contact between the control gate and the floating gate shown in Fig 1(a), the other is stacked cell structure shown in Fig. 1(b). Dummy cell is used for Fowler-Nordheim Constant Current Stress (FN-CCS) and Direct-Current Current-Voltage (DCIV) test; stacked cell is used for Program /Erase (P/E) cycling. Width and length of the test samples are 1um/1um (W/L) for Fig. 1(a) and 0.15um/ 0.15um for Fig. 1(b) respectively. Different UV-state V_t dummy cells and stacked cells have the same oxide thickness but in different p-well concentrations.

Results and Discussions

PART 1: The Results of FN-CCS

The voltage separation shown in Fig. 2 was obtained according to [1], and we find that the trend of V_t, V_{ot} and V_{it} shift after FN-CCS for the higher and the lower UV-V_t are different. The positive Vit shift indicates an increase of acceptor-like Nit while the negative Vot shift at low injected charge indicates positive Not dominates at low charge fluences. A saturated Vot shift observed at about 0.5 C/cm² means that a compensation mechanism of positive and negative N_{ot} does exist. Fig. 3 shows that the higher V_t dummy cell has a larger Subthreshold Swing (S.S.) distortion than the lower V_t one does after stress. From Fig. 4, G_m versus dummy \dot{V}_G , the higher V_t dummy cell degrades more than the lower one at each injected charge. In Fig. 5, the degradation of S.S. and the value of G_{m. max} of the higher V_t dummy are more severe than the lower V_t which implies the higher V_t dummy creates more interface traps than does the lower V_t one during FN-CCS. According to Fig. 2, N_{ot} and N_{it} for the higher and the lower Vt dummy cell were extracted as shown in Fig. 6. It is obvious that the lower Vt dummy cell generates not only less Nat but also less N_{it} than does the higher V_t one during FN-CCS. <u>PART 2: The Results of DCIV</u>

Fig. 7(a) and 7(b) show experimental DCIV results of linear I_B and logarithmic I_S as the function of V_{GB} . From the position of the $I_{B,pk}$ we know that the primary degradation region in our dummy cell during FN-CCS was mainly concentrated on the channel region instead of the S/D extension region. Since we know that the I_{B} value is linearly proportional to Nit, the higher Vt dummy cell generates more N_{it} than the lower V_t one. Fig. 8 also tells the same fact like Fig. 7, and its rising kinetic trend also correlates well with Fig. 6, N_{it} extracted from the mid-gap voltage shifts [1].

From the inset of Fig. 8, the degradation kinetics could be deduced, which based on the four Auger-Impact pathways shown in Fig. 12 (the programming cell, step1~4) [2]. The kinetics consist two behaviors, the linear first-order and the nonlinear second order that starts off around 2C/cm² as seen in the inset of Fig. 10. The key feature of degradation kinetics is the inclusion of the increasing hole concentration with increasing concentration of the interface traps in the negative charge state. From the inset, I_B values will saturate at higher charge fluences (>1~2C/cm²). This is because the generation and annihilation of Nit will reach a steady-state balance to make the net generation of N_{it} zero, then N_{it} will become a constant or a stress time independent, therefore N_{it} will no longer increase and IBpk will reach a nearly constant value.

PART 3: The Results of P/E Cycling Endurance

It is manifest from Fig. 9(a) and 9(b) that the degradation of the programmed state V_t of the higher $UV-V_t$ cell is serious than the lower $UV-V_t$ one. Significant V_t window closure for the higher UV-V_t cell means more serious oxide degradation which leads to tunneling insufficiency. During cycling, both the reduction of the injection field and the increase of the electron trapping sites in the oxide will raise V_t for programmed cells. Not only from Fig. 10(a) and (b) can we find the current degradation but the S.S. distortion degree (shown in the inset) of the higher UV-V_t cell is more severe than that of the lower one. From Fig. 11 the statistical results, the average result for the higher UV-Vt cell is 3K but for the lower UV-Vt cell is 30K. This consequence is clearly shown that the lower UV-V_t cell does prevail over the higher UV-Vt cell in cell reliability.

Modeling and Conclusions

In Fig. 12, four interband Auger recombination and generation processes (step 1~4) are shown. This process requires the presence of two electrons and one hole, or two holes and one electron in the vicinity of each other. Energy conservation is maintained via these forces as one-electron drops into a hole and the recombination energy is carried away by the second hole via Coulomb repulsion. The probability of having two holes next to each other mainly comes from a high acceptor dopant impurity, p-well concentration; in other words, lower UV-Vt has less hole quantities than the higher one. Consequently, the degradation of the higher $UV-V_t$ cell is more serious than the lower $UV-V_t$ one during P/E cycling.

From the aforementioned dummy cell and stacked cell experimental results such as FN-CCS, DCIV and P/E cycling test, the most critical factor of the flash memory cell, UV-V_t, has been thoroughly researched for the first time and the consequence can be easily realized in the latest state-of-the-art flash memory production and industry.

Reference [1] Young-Bog Park et al, in IEEE Trans 1998, pp.1361-1368. [2] C.T. Sah, FSSE-SG, pp.400.



Fig. 1 Schematic diagrams of the test set up for FN CCS, DCIV and P/E cycling by using dummy gate and stacked gate structure.



Fig. 2 V_t and the separated V_{ot} and V_{it} shifts after FN CCS ubder gate injection for the higher and the lower Vt dummy cell.

11

0.5

-0.9

-1

-1.5

0.01

Shift (V)

Voltage 3

Vi

VI

0.1

Injected Charge (C/cm²)



Fig. 5 Subthreshold swing (S.S.) and the initial values for the higher and the lower V_t between two different V_t dummy cells. dummy are 106 and 101 respectively.



0.5

-1

-1.5

10

Fig. 3 I_D -V_G curves(V_D=0.1V) of the higher and the lower Vt dummy and their S.S. after FN CCS at different charge fluence.



Fig. 4 Transconductance versus dummy gate voltage after FN-CCS at different charge fluence.

Jate -4

-4 -3 -2 Gate to 5-----

1.1E-1 1.0E-1 9.0E-1 8.0E-1 7.0E-1 6.0E-1 5.0E-1 4.0E-1 3.0E-1 1.0E-1

-6 -5

Bulk Current, I _B (A)

to Bulk Voltage, V_{GB} (V) -3 -2 -1 0 1 2

-1 0

2

1 3

. (V)

3



Fig. 6 Oxide-trapped charge (Not) and intermaximum Gm shifts after FN CCS. The S.S. face trap charge (N_{ti}) density comparison



Fig. 7(a) Fig. 7(a) and 7(b) show the experimental results of linear bulk current I_B and logarithmic source current I_S versus gate voltage at the forward bias V_{PN} =0.4V at each charge fluence kinetics, which involves the hot hole after FN CCS for the higher, (a), and the lower Vt , (b), dummy cell.



Fig. 8 DCIV maximum I_{B} values for the two different Vt dummy cells after FN CCS. The inset implies the interface trap generation Interband Auger generation mechanism.



Fig. 11 Statistical results of P/E cycling for the higher UV-Vt and the lower UV-Vt cell, which were judged by 0.5V Vt shift of the programmed memory cell.



Fig. 12 Transition Energy Band diagrams of -ration processes are labeled from 1 to 4.

Fig. 9(b) Fig. 9(a)



the corresponding S.S. for (a) the higher UV-Vt cell and (b) the lower UV-Vt cell.