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# Effect of Compensation Implant in SONOS Flash EEPROMs

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## 1. Introduction

SONOS flash EEPROMs are predicted to be the key non-volatile memories for embedded applications due to their ease of fabrication, easy integration with CMOS logic process, and low power operation, apart from the multi-bit storage capability [1,2]. Threshold adjust implants are used to separately adjust threshold voltages ($V_{TH}$) of logic and memory devices, when they are integrated. Memory cells employ a compensation implant to reduce their natural $V_{TH}$. This paper explores the effect of compensation implant on the operation and reliability of SONOS memory cell, through experiments and simulations.

## 2. Results and Discussion

Measurements were done on stack-gate SONOS memory cells with ONO thickness of 5.8/8/6 nm and drawn gate length (L) of 0.25 μm. Fig.1 shows the schematic of the cells used, and their doping schemes. Program and erase (P/E) were done through injection of channel hot electrons and band-to-band tunneling induced hot holes, respectively [1]. Process and device simulations were done in ISE TCAD's DIOS and DESSIS respectively [3]. A full-band Monte Carlo simulator [4] (SMC) was used (after DESSIS) to simulate hot carrier distributions in the channel.

Fig. 2 shows the P/E transients of compensated and normal cells, under similar bias conditions. Program speed is highly degraded in compensated cell even though it has lower $V_{TH}$ (Fig. 1). Compensation reduces the lateral fields near drain junction resulting in lower heating of electrons and a lower program speed. As shown in Fig. 2, use of halo implants can improve program efficiency by making the junction more abrupt (however, they also increase $V_{TH}$). Fig. 3 shows SMC simulated hot electron density and vertical field along the channel, for virgin cells with and without compensation. Compensation reduces peak hot electron density and slightly broadens the profile. On the other hand, erase speed does not show significant dependence on compensation and halo.

The effect of trapped charge (in ONO) on IV characteristics (reverse read [1]) is studied next using simulations. Here, the charge is placed at Si-$SiO_2$ interface above gate-drain overlap and channel in packets (Fig. 1). Increasing channel charge spread increases SS when charge is highly localized, and increasing overlap charge magnitude degrades IV slope in linear region [5,6]. Figs. 4 and 5 show the effect of a given charge on SS, $V_{TH}$ and linear slope to be higher in normal cells compared to cells with compensation. These clearly indicate that compensated cells need higher charge trapping for similar $V_{TH}$ shifts.

Fig. 6 shows the evolution of IV characteristics during program and erase, in compensated and normal cells. Compensated cells show a higher degradation of sub-threshold slope (SS) during programming. However, both the cells recover their SS after erase, showing that localization of trapped charge (and not creation of $N_{IT}$) causes SS degradation during program [5,6].

Compensation is also shown to increase drain disturb in scaled (lower L) SONOS cells due to a higher source-drain (S/D) leakage current (larger SS and lower $V_{TH}$) [7]. Fig. 7 compares drain disturb between normal and compensated cells at a fixed $V_D$. Disturb is much higher in compensated cells but is drastically reduced when S/D leakage is eliminated by floating the source terminal during disturb. Halo reduces S/D leakage but increases the disturb component arising from BTBT induced holes [7].

Fig. 8 shows P/E cycling window for cells with different doping schemes (cells with only compensation are not shown due to their slow programming). Under similar bias voltages, normal cell shows better endurance than the cell with compensation and halo (both are better than cell with halo only). Figs. 9 and 10 show the pre- and post-cycling charge pumping (probes channel region [6]), and GIDL (probes overlap region [6]) characteristics for compensated (with halo) and normal cells. Compensated (with halo) cell shows higher interface degradation in channel (higher $\Delta I_{CP}$) with cycling, which could affect the cell retention. However, GIDL characteristics suggest that compensation and halo have less effect on degradation in overlap region.

## 3. Conclusions

Compensation implants used to reduce the natural $V_{TH}$ of memory cells are shown to a) decrease program speed by lowering electron heating, and reducing effect of trapped charge on cell $V_{TH}$, and b) lead to higher program-state drain disturb at lower L. While introduction of halo increases program speed, it is also shown to result in a higher interface degradation compared to normal cell, after P/E cycling under similar bias conditions and $V_{TH}$ window.

## Acknowledgements

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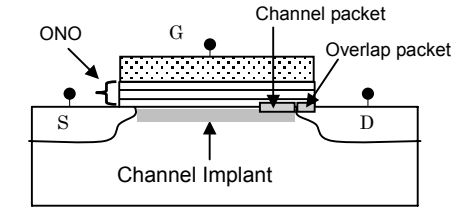
## References

[1] B. Eitan *et al.*, *Proc. SSDM* (1999) 522. [2] C. T. Swift *et al.*, *IEDM Tech. Dig.* (2002) 927. [3] ISE TCAD Manuals, Release 8.0. [4] J. D. Bude *et al.*, IEEE TED **47** (2000) 1873. [5] L. Larcher *et al.*, IEEE TED **49** (2002) 1939. [6] P. R. Nair *et al.*, *IEDM Tech. Dig.* (2004) 403. [7] P. B. Kumar *et al.*, *Proc. IRPS* (2004) 186.




| Device | Channel implant | Typical $V_{TH}$ |
|---|---|---|
| Normal | B | 2.3 V |
| Compensated | B, $BF_2$, As | 1.0 V |
| (in both, halo increases $V_{TH}$ by ~ 0.7 – 1 V) | | |

Fig. 1. Schematic of the SONOS cell used, showing the location of charge packets used in simulations. The channel implants and the typical $V_{TH}$ values are also shown.

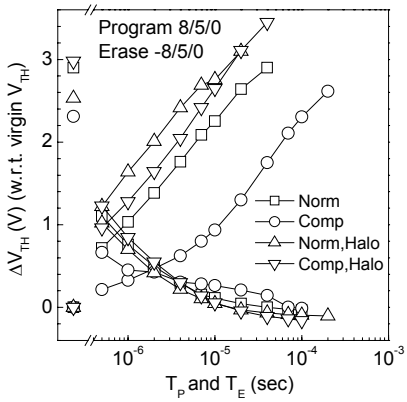



Fig. 2. Program and erase transients of normal and compensated SONOS memory cells with and without halo.

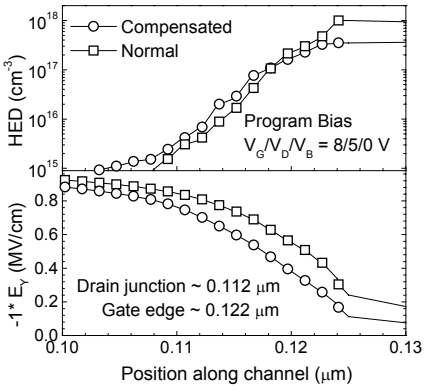



Fig. 3. Simulated hot electron distribution and vertical field along the channel of a virgin SONOS cell under program bias.

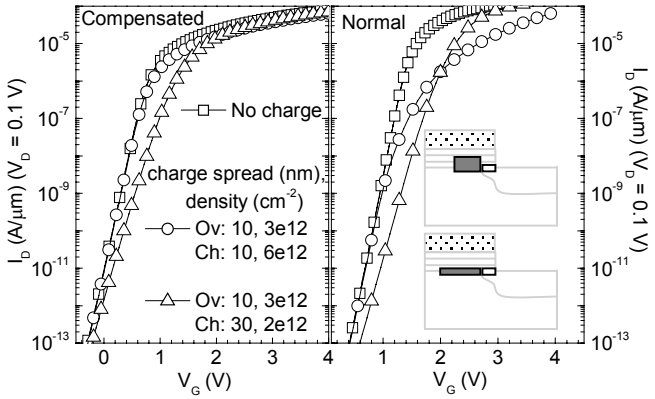



Fig. 4. Simulated IV characteristics showing the effect of varying channel charge spread with overlap charge fixed.

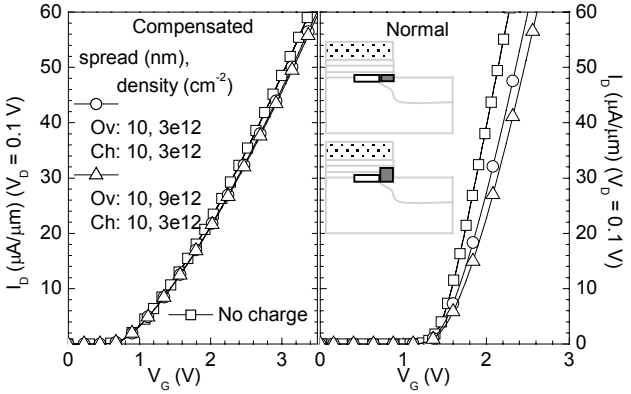



Fig. 5. Simulated IV characteristics showing the effect of varying overlap charge magnitude with channel charge fixed.

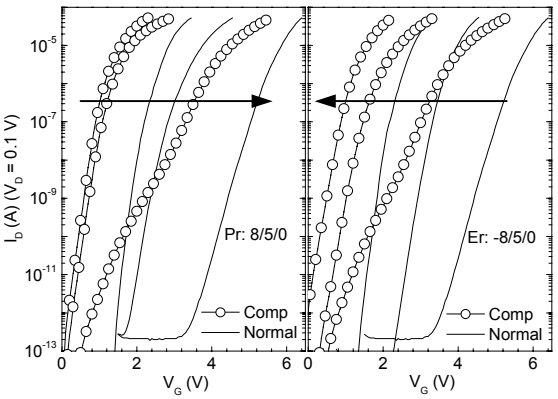



Fig. 6. IV characteristics measured (reverse read [1]) during the P/E transients shown in Fig. 2.

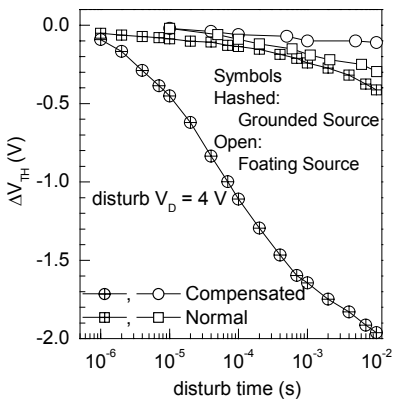



Fig. 7. Drain disturb transients in programmed ($\Delta V_{TH}$ = 2 V) SONOS cells with and without compensation.

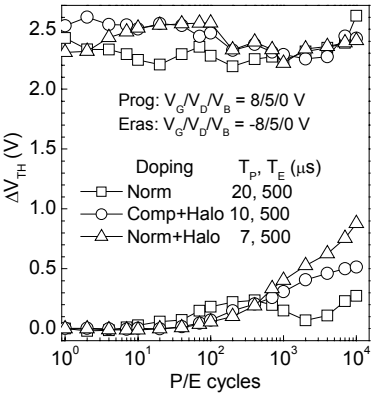



Fig. 8. Endurance of SONOS cells with and without compensation under similar bias conditions.

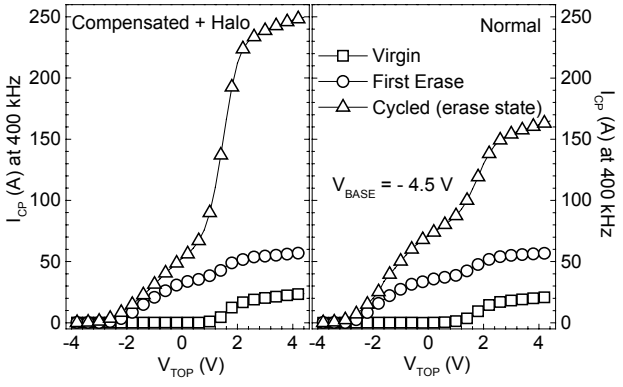



Fig. 9. Pre- and post-cycling (Fig. 8) CP characteristics.

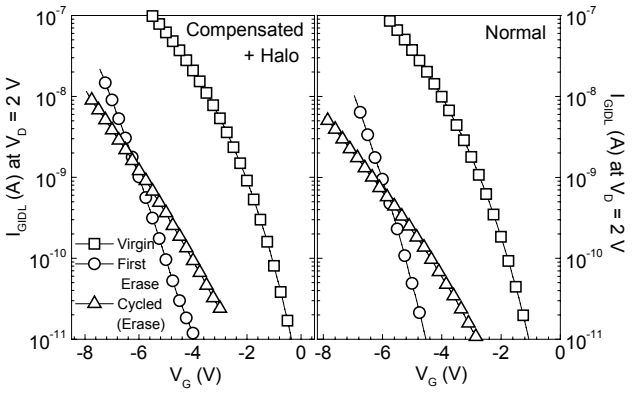



Fig. 10. Pre- and post-cycling (Fig. 8) GIDL characteristics.