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Non-volatile Al_2O_3 memory using an Al-rich structure as a charge storage layer

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1. Introduction

The new SONOS (silicon-oxide-nitride-oxide-silicon) trap memory devices [1-3] have recently been attracting increasing attention because of their potential for low-voltage-writing operation and for extremely large-scale integration due to their thin tunnel insulator. However, several problems remain, one of which is that the number of trap sites is not sufficient in memory cells whose length is shorter than 45 nm. This results in a small change of the threshold voltage between writing and erasing operation, which leads to inadequate data retention. To resolve this problem, we propose a novel non-volatile Al_2O_3 memory using an Al-rich structure as a charge storage layer. This achieves low-voltage writing operation, such as 7 V, due to the Al-rich structure. Also, this memory is easy to fabricate because we only need to prepare Al atoms. In this article, the fabrication and characteristics of our new memory device are described.

2. Device fabrication

The cross section of the structure of the device is shown schematically in Fig. 1. We used (100) p-type Si ($\rho = 2$ Ωcm) wafers. As a tunnel barrier insulator, 4.5 nm of Al_2O_3 was deposited using electron cyclotron resonance (ECR) sputtering. Next, 4.5 nm of Al-rich Al_2O_3 was deposited as a charge storage layer. For fabrication of the Al-rich structure, the O_2 gas flow rate was decreased from the normal value, which is discussed in the next section. Next, 15 nm of Al_2O_3 was deposited as a blocking barrier insulator. After deposition, the sample was annealed in about 3×10^{-7} Torr at 550 $^{\circ}$C to obtain good insulator characteristics.

3. Results and discussion

Fig. 2 shows the O_2 flow rate for fabricating stoichiometric Al_2O_3 and Al-rich Al_2O_3 by ECR sputtering [4]. When the O_2 flow rate is smaller than 4 sccm, the refractive index measured using 623.8-nm light is much larger (1.7 - 2.4) than the stoichiometric Al_2O_3 value. To deposit Al-rich Al_2O_3, we used a 2.5-sccm O_2 flow rate in this experiment. Fig. 3 shows the etching time of 50-nm-thick Al_2O_3 in the case of a 0.25% HF etchant as a function of O_2 flow rate. It is clear from Fig. 3 that Al-rich Al_2O_3 fabricated with the reduced O_2 flow rate has the characteristic somewhere between Al and Al_2O_3.

We measured the high-frequency capacitance-voltage (C-V) characteristics of an Al-rich Al_2O_3 sample with a length of 200 μm at 1 MHz. As shown in Fig. 4, clear hysteresis is observed with a 3.2-V hysteresis voltage window (ΔV) when the applied voltage is 7 V. From this ΔV, the electron trap density is estimated to be

1.0×10^{19} cm^{-3}, which is 1.5 times larger than that of SONOS [5]. The experimental insulator capacitance value is about 120 pF. Theoretically, insulator capacitance C is written as $C = \varepsilon \cdot S/d$, where S is the cell area and d the insulator thickness. Here, S is (200 μm)^2 and d is 24 nm. Then, C is estimated to be 130 pF. This value is very close to the experimental one.

Next, we investigated the memory cell size dependence of C-V hysteresis. In Fig. 4, we define the states of large and small capacitance when the gate voltage is 0 V as states H and L, respectively. We fabricated several memory cells with lengths of 200, 150, 100, 50, or 20 μm. States H and L as a function of memory cell area are shown in Fig. 5. They change in proportion to S, which means this device is well explained by MIS theory in both writing and erasing operation.

Figs. 6 and 7 show C-V characteristic of the device using stoichiometric Al_2O_3 (5.5-sccm O_2 flow rate) and Al-rich Al_2O_3 (2.5-sccm one) as a charge storage layer when 5 V is applied. The ΔV is almost zero in the stoichiometric Al_2O_3, while it is 1.6 V in Al-rich Al_2O_3. Fig. 8 shows the change of ΔV as a function of the applied voltage. It is clear that the Al-rich Al_2O_3 film shows large hysteresis compared with the stoichiometric Al_2O_3 one.

Finally, the data retention is investigated. In Fig. 9, the horizontal axis is time and the vertical one is the capacitance values of states H and L of a 50-μm-length memory cell when the applied voltage is 7 V. The capacitance values showed almost no change after 2 hours, which strongly indicates that this memory will stay non-volatile for several years or more. This good retention is explained by the fact that the barrier height of Al_2O_3 is large compared with that of Si_3N_4. This means Al_2O_3 film is more suitable for the use in high-temperature conditions than Si_3N_4 film.

4. Summary

In summary, we proposed a novel non-volatile Al_2O_3 memory that is easy to fabricate. Large C-V hysteresis can be obtained using Al-rich Al_2O_3 as a charge storage layer. The electron trap density of the charge storage layer in this experiment was 1.5 times larger than that of SONOS. Data retention is good, and this device will stay non-volatile for several years or more.

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References
[1] T. Sugizaki et al., Symp. VLSI Tech. Dig. (2003) 27.
[2] C. H. Lee et al., IEDM Tech. Dig. (2003) 613.
[3] Y. N. Tan et al., IEDM Tech. Dig. (2004) 889.
[4] Y. Jin et al., J. Vac. Sci. Technol. B **21(3)** (2003) 942.
[5] S. Minami et al., IEEE Trans. **ED-38** (1991) 2519.

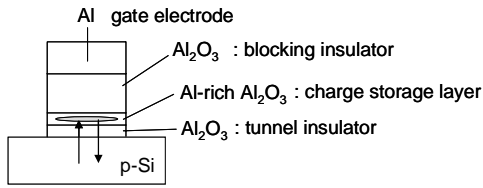Fig. 1 Schematic cross section of Al$_2$O$_3$ memory using an Al-rich structure.

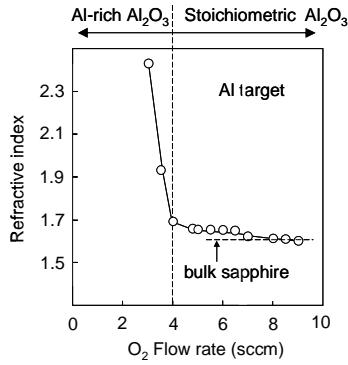Fig. 2 The region of stoichiometric Al$_2$O$_3$ and Al-rich Al$_2$O$_3$ as a function of O$_2$ flow rate.
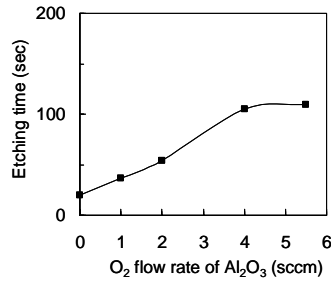
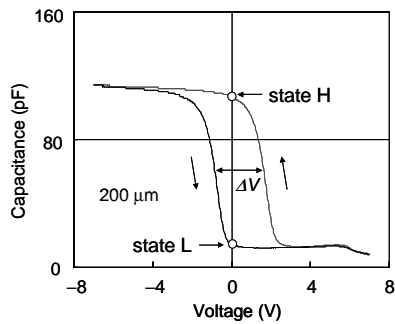Fig. 3 The etching time of Al$_2$O$_3$ as a function of O$_2$ flow rate.

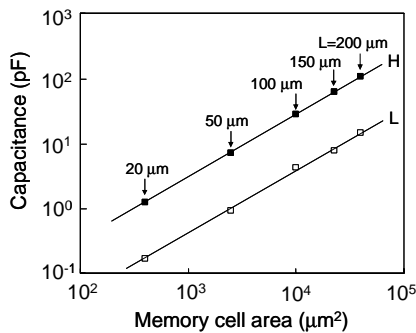Fig. 4 C-V hysteresis of Al-rich Al$_2$O$_3$ film when 7 V is applied.

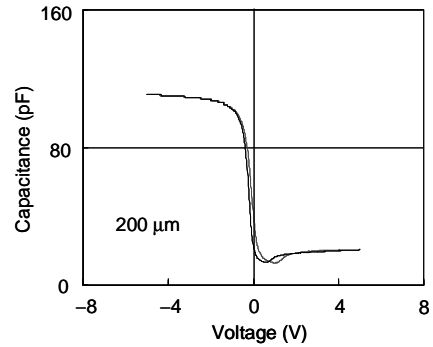Fig. 5 Capacitance values of states H and L as a function of memory cell area.

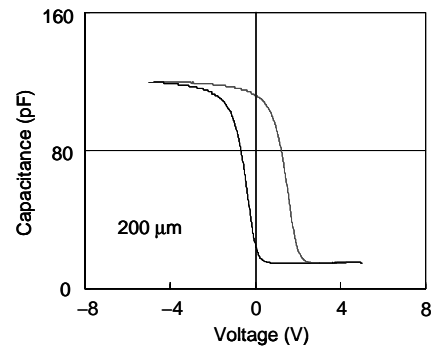Fig. 6 C-V hysteresis of stoichiometric Al$_2$O$_3$ film when 5 V is applied.

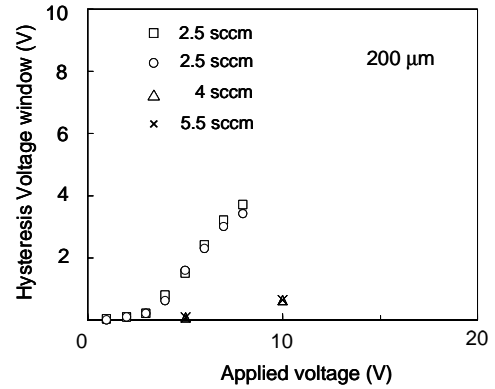Fig. 7 C-V hysteresis of Al-rich Al$_2$O$_3$ film when 5 V is applied.

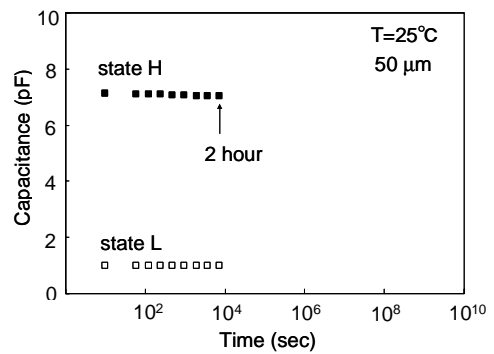Fig. 8 C-V hysteresis voltage window as a function of the applied voltage.

Fig. 9 Data retention.