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P4-8 A new low temperature APM cleaning process to improve ONO integrity in 0.18μm stacked-gate EEPROM memory

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Introduction

Inter-poly dielectric thickness dominates program/erase speed and the amount of read current for a nonvolatile memory cell transistor with a stacked-gate structure. Oxide-Nitride-Oxide (ONO) stacked film has been widely used as an inter-poly dielectric in stacked-gate flash EEPROM devices for the improvement of the reliability problem due to the degradation of data retention capability occurring during the long-term memory operation [1,2]. ONO has been reported to show high breakdown voltage and low defect density. There are many factors, which affect the quality and uniformity of ONO film during the process. In the present study, low temperature APM (LT-APM) clean (<50ºC) is the 1st time introduced as the cleaning process after ONO deposition to improve the integrity of ONO film. The typical clean after ONO deposition before high voltage gate oxide growth is the normal APM (N-APM) also commonly known as SC1 clean, it is a mixture of $NH_4OH/H_2O_2/H_2O$ at temperatures between 70 and 90ºC[3]. The purpose of the APM clean is to remove organic particles. It was reported in the literature that SC1 process has an impact on surface roughening [4], yield loss due to the degradation of dielectric breakdown [5], etching of silicon [6], and oxide loss [7]. In our study, it has been found out that better ONO integrity with less surface roughness, better uniformity, hence, longer Time Dependent Dielectric Breakdown (TDDB) and stable ONO thickness have been achieved by using this LT-APM clean. Further study found out that the temperature of the APM play a dominant role in the roughness improvement, instead of the concentration of the chemical.

Experimental

All the devices studied in this work were fabricated using 0.18μm CMOS EEPROM technology. The ONO stack separates the floating gate and the control gate. It consists of a layer of SiO_2 at the bottom, a Si_3N_4 layer in the centre and another SiO_2-layer on top. The SiO_2 is deposited as High Temperature Oxide (HTO) at 780ºC. The basic process related with ONO deposition is shown in Fig 1. A Flash cell starts with tunnel oxide at the bottom, followed by the floating gate poly and ONO deposition. Subsequently, poly etch is done to grow high voltage gate oxide. A clean step is introduced before control gate poly deposition to clean the top oxide of ONO. Comparison between LT-APM and N-APM and their effects on ONO were studied. The composition, temperature and process time of N-APM and LT-APM used in this study are summarized in Table 1.

Results and Discussion

The etch rate of silicon dioxide in the APM clean depends on the NH_4OH concentration, the temperature and lifetime of the batch. Fig.2 shows that the oxide loss in LT-APM is significantly lower than N-APM. It is also observed that the incremental loss with dip time is much lesser for LT-APM, which means less variation during the chemical lifetime for LT-APM. This observation is further verified by the TEOS oxide loss during the chemical lifetime in Fig 3. Due to the difference in oxide loss between N-APM and LT-APM, the top oxide thickness needs to be adjusted to maintin the same electrical ONO thickness. TDDB tests have been conducted on 2 smaples with the same thickness of ONO at 19 V and 18 V. LT-APM clean shows 1 order longer breakdown lifetime than N-APM in Fig 4 and Fig. 5. The previous studies indicate that the trapped electrons at the interafce between Si_3N_4 and bottom oxide[8], trapped holes in the top oxide layer [9] , and current enhancement at defects in the bottom oxide films struck by accelerated electrons from the Si_3N_4 layer[10] are attributed to the breakdown of the ONO film. In this case, this LT-APM is only applied to the top oxide, it has no impact on the interface of bottom oxide and Si_3N_4. The top oxide thickness for both N-APM and LT-APM clean are above 30 Å, as to the trapped hole condition, there should be equivalent[11]. Another candidate to dominate the dielectric breakdown of ONO films is an effect of the local thinning of film thickness due to surface roughening. Fig. 6 shows oxide film using LT-APM clean only has half of the roughness of N-APM clean, which can explain the better TDDB result for LT-APM clean.The wafer map on the electrical ONO thickness also shows more uniformity across the wafer for LT-APM clean (Fig 7). It is good to maintain better Cpk performance and also helpful for those EEPROM products, whose yield are sensitive to Vt window (Programme Vt – Erase Vt), to keep a stable yield, as electrcial ONO thickness is one of the main factors impacting EEPROM Vt window. In order to find out the main factor causes the less surface roughning and unformity improvement, the saturation curves for NH_4OH and H_2O_2 were monitored during the lifetime as shown in Fig 8 (a) and (b). Suprisely, for LT-APM, the conconceration of NH_4OH is higher than N-APM during the whole lifetime. Typically, the oxide etch rate of APM increases with OH^- concentration, but our measurement in Fig. 1 shows much less oxide etch rate for LT-AMP, hence, the temperature of the LT-APM is the dominant factor to suppress the oxide etching and surface roughening, rather than the diluted concentration listed in Table 1.

Conclusions

A novel LT-APM clean after ONO film deposition has been adopted in 0.18μm CMOS EEPROM technology and the effects of this LT-APM clean on the integrity of ONO has been examined. This new LT-APM clean process after ONO film deposition achieves less oxide loss and less surface roughness by comparing with the typical N-APM clean, subsequently, it results in the better and stable electrical ONO thickness and better TDDB results of ONO. The yield for this LT-APM clean process is better (due to less fluctuation of electrical ONO) or equivalent to that obtained with N-APM. This verified that the LT-APM did not have a negative impact on defect density with respect to that of N-APM.

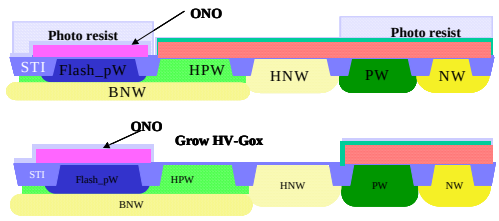


Fig. 1 Schematic of ONO related process flow

Table 1. Chemical and their composition, temperature and process time used in this study.

Chemical	Temp (°C)	Intial ration (volume) NH4OH:H2O2:DIW	Process time (s)
N-APM	50-70	`1:4:20	600, 1200, 1800
LT-APM	<50	`1:2:50	300, 600, 1200, 1800

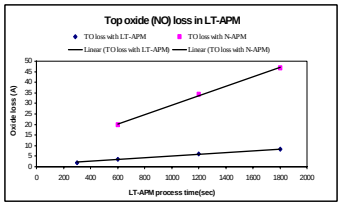


Fig. 2 Etch rate check of N-APM and LT-APM. The oxide loss in LT-APM is significantly lower than N-APM. More important, the incremental loss with dip-time is much lesser in LT-APM

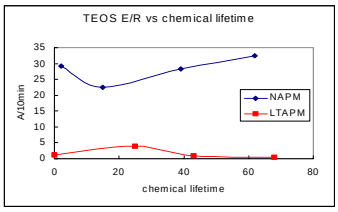


Fig. 3 TEOS E/R comparison between N-APM and LT-APM during chemical lifetime.

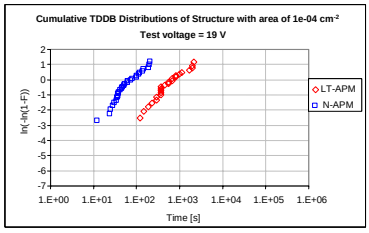


Fig. 4 TDDB data of ONO film with LT-APM clean and N-APM clean. The test voltage is 19 V,

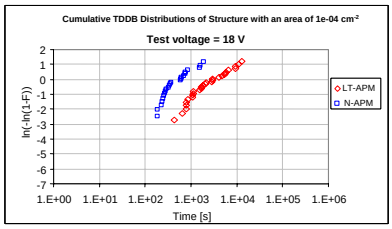
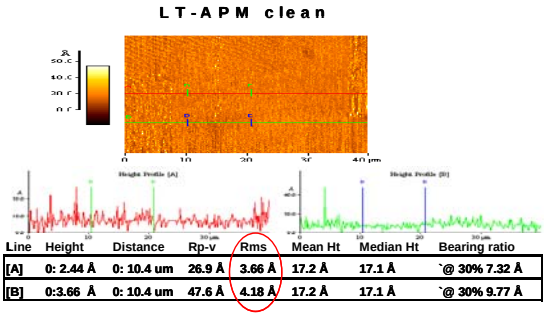


Fig. 5 TDDB data of ONO film with LT-APM clean and N-APM clean. The test voltage is 18 V



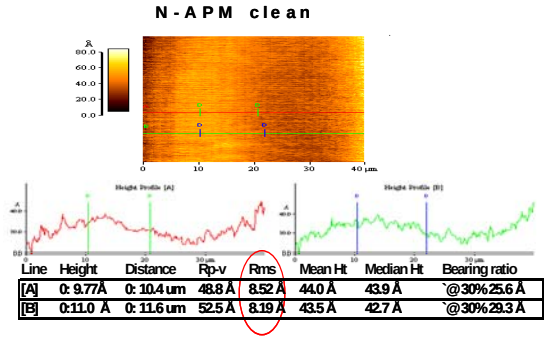


Fig. 6 surface roughness comparison between LT-APM clean and N-APM cleaning, showing only half of the roughness of LT-APM comparing with N-APM.

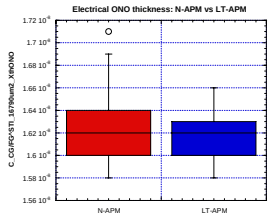


Fig. 7 within wafer uniformity on electrical ONO thickness comparison between LT-APM clean and N-APM clean, showing more within wafer uniformity for LT-APM clean.

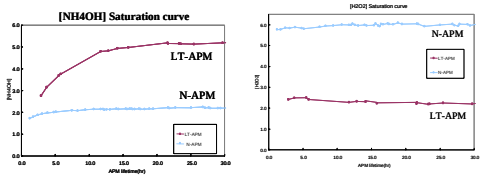


Fig. 8 (a) NH_4OH Saturation curve during APM lifetime, showing much higher OH^- in LT-AMP than N-APM; (b) H_2O_2 Saturation curve during APM lifetime.

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