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Effects of Voltage Cycling on Polarization and Reliability of 3D SBT Ferroelectric Capacitors Integrated in 0.18μm CMOS Technology.

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1. Introduction

Ferroelectric memory (FeRAM) offers important advantages over other non-volatile memories as low-voltage/low-power operation, fast write, and byte addressability. One concern towards scaling is its charge-based operation and limited polarization, requiring the development of 3D structures [1].

Our pseudo 3D ferroelectric capacitor (FeCAP) cell was previously demonstrated in a 0.35μm technology [2]. $SrBi_2Ta_2O_9$ (SBT) is used because of its excellent reliability properties [3]. Recently, we developed the scaled cell integration technology in 0.18μm CMOS. In this work, we report on electrical and reliability characteristics of our 3D FeCAP integrated in 0.18μm technology. In particular, effects of bipolar (fatigue) and unipolar (dynamic imprint) voltage cycling are explored.

2. Integration of 3D FeCAP Cell in 0.18μm Technology

The integration of the 3D FeCAP on top of CMOS consists of following steps: (1) deposition of Pt/IrO_2/Ir/TiAlN Bottom Electrode (BE) / O_2-barrier stack on top of W contact plugs, (2) dry-etch patterning of the BE stack, (3) MOCVD deposition of SBT followed by crystallization anneal (700°C, 1h, O_2), (4) Pt Top Electrode (TE) deposition, (5) dry-etch patterning of TE and SBT, (6) H-seal and isolation deposition, followed by CMP, (7) formation of W-contacts of M1 to Si and to Pt Plate Line, and (8) Al metallization. Critical issues for scaling to 0.18μm are control of the lateral oxidation distance of the TiAlN layer and formation of the deep M1 to Si contacts. Fig. 1 shows the integrated cell in the Bit Line direction. The Pt TE is used as Plate Line and covers the FeCAP sidewalls in the other direction (Fig.2).

3. Hysteresis and 3D Effect

The hysteresis of integrated 3D capacitors shows an increase of Pr value of 70% compared to 2D reference capacitors (Fig.3). Still, the sidewall contribution is only 60% of what could be geometrically expected, in agreement with 0.35μm results [4]. The limited sidewall contribution maybe explained by different SBT material composition at the sidewalls [4] while also mechanical stress effects may play a role as a change in lattice parameters has been observed [5].

4. Reliability and Effect of Voltage Cycling

Fatigue Cycling

A typical reliability limitation in FeRAM is Pr degradation during R/W cycling. Therefore, fatigue of our capacitors was tested by applying bipolar switching pulses. No degradation occurred up to 10^{13} cycles, and even a small increase of 2.Pr (=Ps-Pns) is observed (Fig.4). For 0.35μm 3D capacitors, similar Pr increase was observed after fatigue, and could be attributed to a wake-up (poling) effect in the SBT sidewall material [4].

Dynamic Imprint

The development of an internal field during data storage may cause imprint failure. The dynamic imprint is a severe imprint test using high temperature stress combined with unipolar voltage pulsing. A gradual field-shift of the hysteresis that is smaller than reported for 2D SBT FeCAPs using less severe stress conditions [6,7] is observed (Fig.5). However, while Pr typically decreases for 2D FeCAPs due to pinning [6.7], we observe a concomitant small gradual increase of Pr. As also for 0.35μm 3D FeCAPs, we reported an improvement of loop squareness during imprint pulses [3], this is another indication of a poling effect of in our 3D FeCAPs that competes with the imprint pinning.

Fatigue Cycling after Imprint

When applying a bipolar “fatigue” stress to a sample that got unipolar “imprint” stress before, interestingly, the hysteresis asymmetry gradually disappears again (Fig.6b). As for the Pr value, an increase is observed (Fig 6a). Similar effects have been reported when cycling a pre-irradiated sample [8]. These resuls indicate a depinning of trapped charge by cycling.

6. Conclusions

3D FeCAPs stacked on W-plug were successfully integrated in 0.18μm technology using MOCVD-SBT. The effective Pr was increased by 70% due to the sidewall contribution. The samples showed no fatigue degradation after 10^{13} R/W cycles, on the contrary, an increase of Pr was observed. Unipolar voltage pulses in dynamic imprint test resulted in limited loop shifting concomitant with a small Pr increase. Bipolar pulsing after this imprint restored the hysteresis asymmetry while Pr further increased. These particular properties are attributed to cycling induced poling/depinning effects in the SBT sidewall material.

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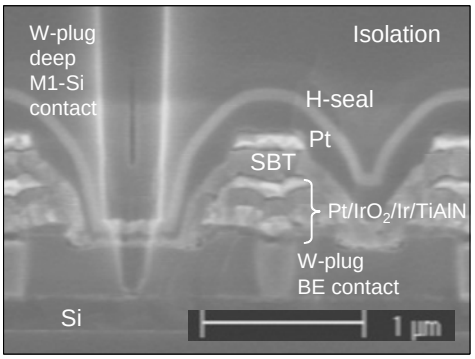

Fig. 1 Integrated 3D SBT FeRAM cell in 0.18µm technology (Bit Line direction)

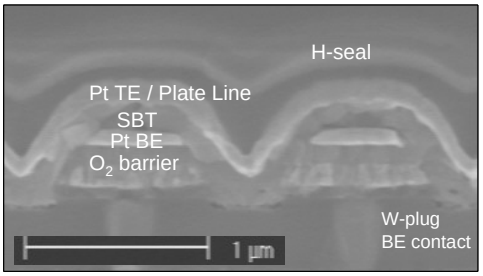

Fig. 2 Integrated 3D SBT FeRAM cell in 0.18µm technology (Plate Line direction, with 3D effect on FeCAP sidewalls)

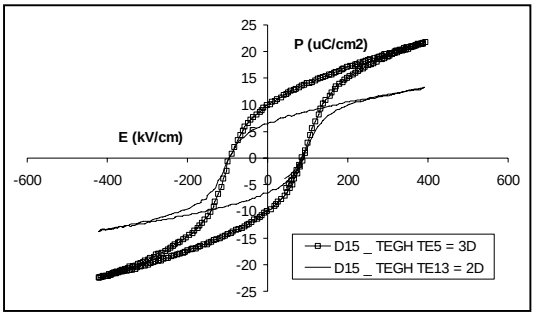

Fig. 3 Hysteresis of 3D vs. 2D integrated FeCAP

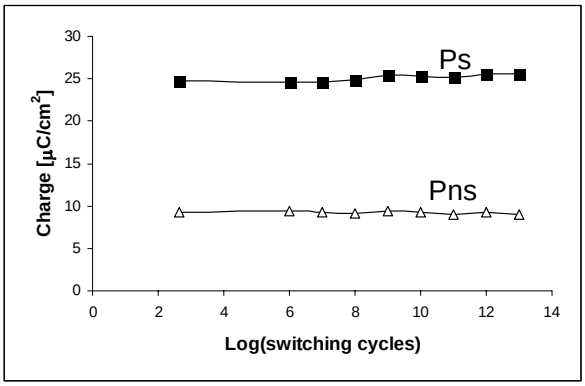

Fig. 4 Fatigue cycling of 3D FeCAP (+/-5V amplitude). The switching polarization Ps continues to slightly increase, while non-swithing Pns slightly decreases up to 10^{13} cycles.

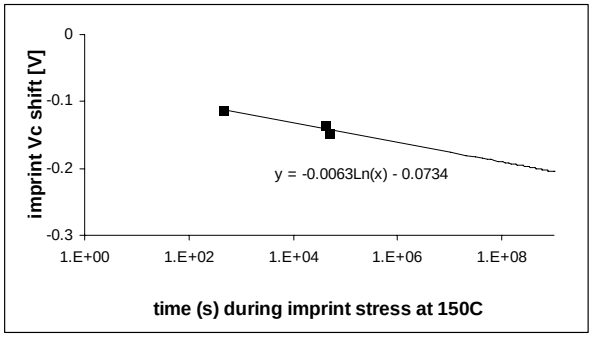

Fig. 5 Shift of coercive voltage V_c of hysteresis loop versus time of dynamic imprint stress (5V unipolar cycling at 10MHz, 150°C).

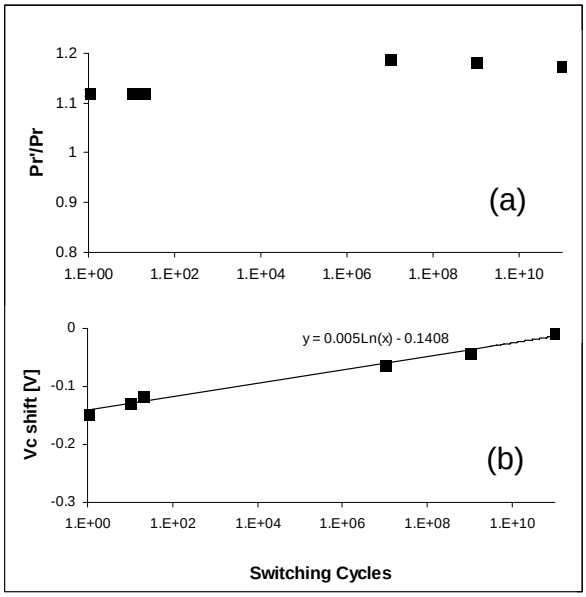

Fig. 6 Pr increase (a) and back-shift of hysteresis loop Vc (b) as function of number of bipolar +/-5V cycles applied to capacitors imprinted with 10^{13} unipolar 5V cycles at 150°C.

References

[1] R.Zambrano, Integrated Ferroelectrics **53** (2003) 247.

[2] D. Maes, J.-L. Everaert, L. Goux, J. Lisoni, V. Paraschiv, M. Schwitters, L. Haspeslagh, D. J. Wouters, C. Artoni, C. Caputa, P. Casella, G. Corallo, G. Russo, R. Zambrano, H. Monchoix, and L. Van Autryve, Integrated Ferroelectrics **66** (2004) 71.

[3] L. Goux, G. Russo, N. Menou, J.G. Lisoni, M. Schwitters, V. Paraschiv, D. Maes, C. Artoni, G. Corallo, L. Haspeslagh, D.J. Wouters, R. Zambrano, and C. Muller, IEEE Trans.El.Dev. **52** (2005) 447.

[4] L. Goux, J.G. Lisoni, M. Schwitters, V. Paraschiv, D. Maes, L. Haspeslagh, D.J. Wouters, N. Menou, Ch. Turquat, V. Madigou, Ch. Muller, R. Zambrano, *submitted for publication*.

[5] N. Menou, L. Goux, J. Lisoni, M. Schwitters, Ch. Turquat, V. Madigou, J-L. Hodeau, Ch. Muller, D.J. Wouters, presented at ISIF 2004, Gyeongju, Korea, April 5-8, 2004.

[6] T.Hase, T.Noguchi, K.Takemura, Y.Miyasaka, Jpn.J.Appl.Phys. **37** (1998) 5198.

[7] M.Grossmann, O.Lohse, D.Bolten, U.Boettger, R.Waser, W.Hartner, K.Kastner, G.Schindler, Appl. Phys. Lett. **76** (2000) 363.

[8] N.Menou, A-M. Castagnos, Ch.Muller, D. Goguenheim, L. Goux, D. J.Wouters,J-L.Hodeau, E.Dooryhee, R.Barrett, J.Appl.Phys. **97** (2005).