Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.670-671

P5-10L

Measurement of Inductive Coupling in Wireless Superconnect

Daisuke Mizoguchi, Noriyuki Miura, Yoichi Yoshida,
Nobuhiko Yamagishi and Tadahiro Kuroda

Keio University, Department of Electronics and Electrical Engineering
3-14-1, Hiyoshi, Kohoku-ku, Yokohama 223-8522, Japan
Phone: +81-45-566-1779 E-mail: {mizo, miura, yoshida, yamagishi}@kuro.elec.keio.ac.jp, kuroda@elec.keio.ac.jp

1. Introduction

3D-stacked System in a Package (SiP) has been investigated for high-performance and high-density packaging in recent years. A wireless interconnect technology utilizing inductive coupling has been reported in [1] to achieve high-speed and low-power inter-chip communication in SiP. Fig. 1 illustrates this scheme. The inductive coupling channel is modeled by an equivalent circuit shown in Fig. 2 and it behaves as a band-pass filter. This equivalent circuit is very simple and does not consider chip stacking. In stacked-chip communication, semiconductive substrate exists between inductors which induces eddy current and reflection at the boundary, as a result, it may degrade signal. However, there is no report on measurement of the effect. In this paper, mutual inductance of inductive coupling is measured and evaluated in actual stacked chips including polishing and thinning effect. In addition, power grid is also measured.

2. Frequency Analysis

In inductive inter-chip wireless communication, communication efficiency strongly depends on vertical communication distance, X, which is given by the sum of the thickness of stacked upper chip and glue layer. The inductor has to be designed considering the chip and glue layer thickness. With given X and layout parameters of inductor, coupling coefficient, k, is calculated by using simple yet accurate model based on the Biot-Savart law [2]. Frequency characteristics of the inductive coupling including parasitic effect are analyzed by the equivalent circuit model in Fig. 2.

3. Experimental Setup

In this paper, measurement results in actual stacked chips are compared with calculations by the model. A test chip was fabricated for measurement. The test chip integrates 150, 200, 250μm-diameter inductors with and without locating power grid (Fig. 1). Fig. 3 shows cross section of stacked test chip. Communication distance X is changed and S21 is measured to verify the proposed coupling coefficient calculation scheme.

The bulk thickness T is changed while keeping X constant to observe the bulk's eddy current effect. In addition, ground mesh effect is measured using a pattern that has ground mesh under the inductor in upper chip. Figure 5 depicts stacked test chips. GND in each chip is connected by silver paste.

4. Measurement Result

The measurement result of communication distance efficiency to S21 is shown in Fig. 5. Figure 5 shows S21 frequency characteristics of each inductor for D=150μm, D=200μm and D=250μm. In each figure, X is changed in steps of 25μm from 50um to 100μm with the calculated result from model in Fig. 2. Measurement result and calculated result shows good agreement in different conditions. From this result, the accuracy of proposed coupling coefficient calculating scheme is confirmed.

Figure 6 shows measurement result of bulk effect evaluation with constant X. In this measurement setup, it is difficult to keep same X under different thick ness of insulator. So, actual X is varied in every stacked chip. In Fig.6, X is 141μm, 125μm and 129μm. The measurement result contains eddy current effect and calculated result does not contain that effect. But, difference between measured result and calculated result is very small under 3 GHz. Eddy current effect does not become a problem for the application of inductive inter-chip communication that its target frequency is currently about 1GHz.

Figure 7 shows ground mesh effect in inductive inter-chip communication. The ground mesh has 30μm pitch, 3μm width. It is rough mesh, but S21 becomes about 10% lower than without the mesh. This result shows that power grid should be removed near the inductive inter-chip communication channel.

5. Conclusions

In this work, measurement of inductive coupling between actual stacked chips is reported. 3 measurement results are reported. The first result shows that proposed coupling coefficient estimation scheme has good accuracy. Next measurement result shows that when we measure S21 by changing bulk thickness T and with constant value of X, we find that the effect of eddy current is very small for inductive inter-chip wireless communication. Finally, ground mesh effect is measured. From this result, we conclude that power grid should be removed near the inductive inter-chip communication channel.

Acknowledgement

The authors are grateful to Masamoto Tago with NEC Corporation for the chip assembly and Muneo Fukaishi and Yoshihiro Nakagawa with NEC Corporation for their assistance in the measurement.

References

[1] D. Mizoguchi, *et al.*, "A 1.2Gb/s/pin Wireless Superconnect based on Inductive Inter-Chip Signaling (IIS)," *ISSCC Dig. Tech. Papers*, pp.142-143, Feb. 2004.

[2] N. Miura, et al., "Analysis and Design of Inductive Coupling and Transceiver Circuit in Inductive Inter-Chip Wireless Superconnect," *JSSC*, vol. 40, no. 4, Apr. 2005, pp.829-837.

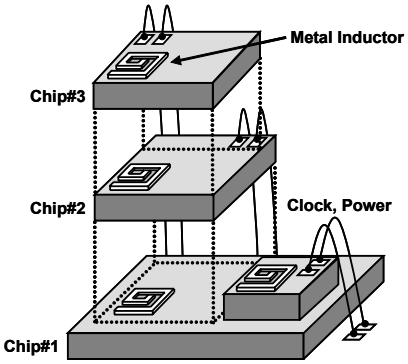


Fig.1 Inductive inter-chip wireless superconnect.

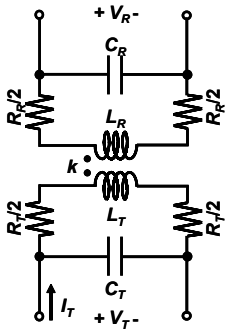
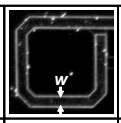
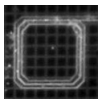


Fig.2 Equivalent circuit of inductive coupling.

Table 1 Layout parameters of metal inductors.

Micro-Photograph				
Diameter, *D* [μm]	150	200	250	150, 200, 250
Width, *w* [μm]	10	10	30	10, 10, 30
Turns, *n*	8	8	4	8, 8, 4
Ground Mesh	No	No	No	Yes

4-Layer Metal Inductor in 0.25μm CMOS

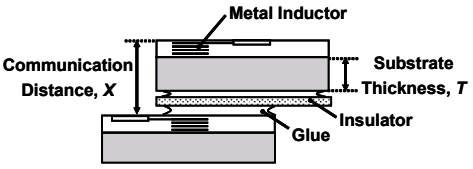


Fig.3 Cross section of stacked test chips and each physical parameter.

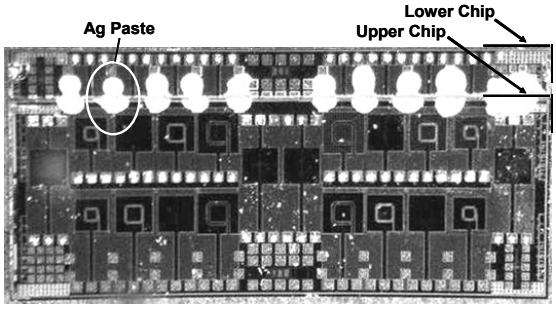


Fig. 4. Microphotograph of stacked test chips with Ag paste for ground connection between upper and lower chips.

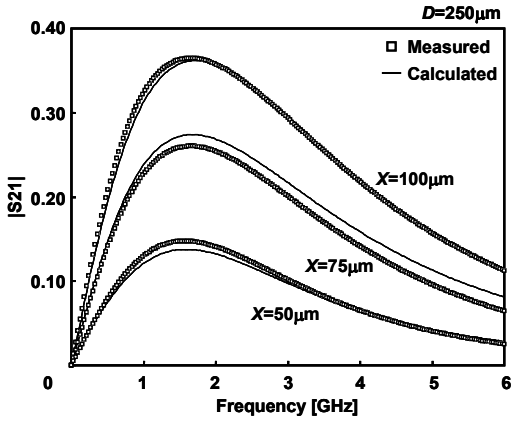


Fig.5 Measured and calculated S21 depending on *X*.

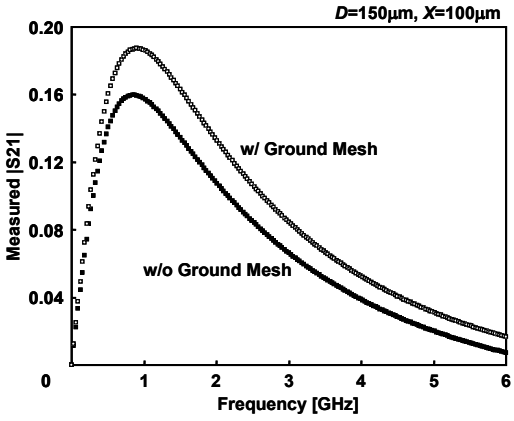


Fig.7 Measured S21 with and without ground mesh.

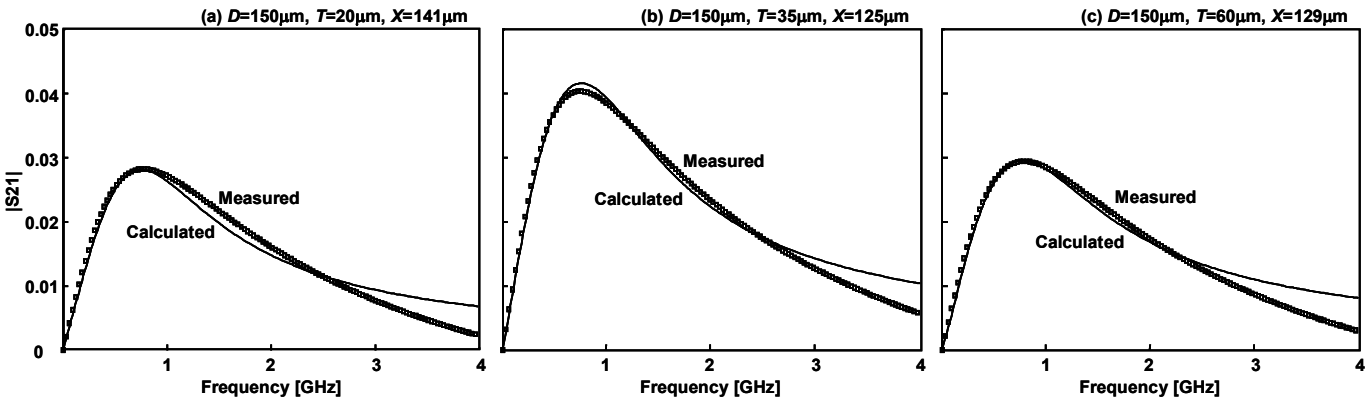


Fig.6 Measured and calculated S21 with eddy current effect depending on substrate thickness, (a) *T*=20μm, (b) *T*=35μm, (c) *T*=60μm.