Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.672-673

P5-11L

A 20% Power Reduction in Two-stage Opamp by Source-Degenerated Active-Load Phase Compensation

Atit Tamtrakarn[1], Koichi Ishida[1] and Takayasu Sakurai[1]

[1]Center of Collaborative Research, Institute of Industrial Science, Univ. of Tokyo
4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, Japan
Phone: +81-3-5452-6253 E-mail: atit@iis.u-tokyo.ac.jp

1. Introduction

An opamp is the most widely used block in analog applications and low-power implementation of opamps is a key for realizing the ubiquitous electronics. The simplest opamp is the conventional two-stage topology [1]-[2]. This opamp provides high output voltage swing, and high DC gain but this topology consumes high power because the output stage consume large current to eliminate instability caused by a right half plane zero in the feed-forward path. This zero can be removed by using RC Miller compensation method, but inserting a resistor in the feed-forward path consumes large area and moreover the design closure becomes difficult because the resistance varies due to process variation. Thus, it is preferable to avoid the resistor. Cascode common-source two-stage topologies can be used in low-voltage design [3]-[4]. These topologies may provide lower power solution but generate two zeros on both side of imaginary axis [4]. These zeros do not degrade phase margin but they increase possibility of pole-zero doublet problem which causes longer settling time. Another approach is to feedback opamp through source node of a common-gate amplifier [5]. This topology needs extra current for the common-gate amplifier and is not suitable for low-power design.

This paper presents a low-power opamp design approach based on a degenerated active-load phase-compensation scheme. The proposed scheme eliminates a feed-forward path in the conventional Miller compensation technique without extra power. The proposed topology is good for low-voltage applications because it does not employ stacked transistors operated in a saturated region. A tested chip is manufactured by using 0.35μm triple-metal double-poly CMOS process. The measurement results confirm that the proposed opamp can save 20% of the power consumption of the RC Miller compensated opamp.

2. Proposed opamp

Fig. 1 shows the conventional opamp and the proposed opamp. The input stage consists of a differential pair with an active load plus degenerated resistors. Transistors M3 operate in a triode region and they are used for degenerated resistors. The output of the input stage maintains high impedance because transistors M2 still operate in the saturated region and high gain can be realized. The output swing is rail to rail. To stabilize the two-stage opamp, phase compensation is necessary. A compensation capacitor, C_C, feeds back a signal from the output node into the source of M2. The signal goes to the drain of M2 through common-gate structure, and then feeds back to the gate of the output transistor. Meanwhile, the inter-stage output signal on the drain node of M2 does not feed forward to the source. Thus, the feed-forward path is eliminated although there is a feed-back path.

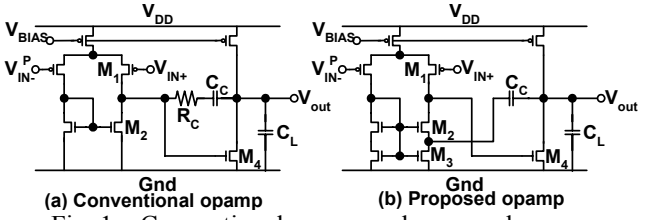

Fig. 1 Conventional opamp and proposed opamp

Let us define transconductance of each transistor in Fig.1 as g_m, output resistance of the input stage as R_{O1}, gate-source parasitic capacitance of each transistor as C_{GS}, and total resistance at drain node of M3 as R_3. The load capacitance and the load resistance are represented by R_L and C_L, respectively. Then, the opamp can be described by a small-signal model in Fig.2. The transfer function of the proposed opamp is obtained from the small-signal model as follows.

$$\frac{v_{OUT}}{v_{IN}} = \frac{A_{DC}\left(1+\frac{s}{\omega_Z}\right)}{\left(1+sk_1+s^2k_2+s^3k_3\right)}, \quad (1)$$

where

$$A_{DC} = g_{m1}g_{m2}R_{O1}R_L,$$

$$\omega_Z = \frac{1+g_{m2}R_3}{C_CR_3} \approx \frac{g_{m2}}{C_C},$$

$$k_1 = C_{GS4}R_{O1} + R_L(C_C+C_L) + \frac{C_CR_3\left(1+\frac{g_{m4}}{g_{m1}}A_{DC}\right)}{1+g_{m2}R_3},$$

$$k_2 = C_{GS4}R_{O1}R_L(C_C+C_L) + \frac{C_CR_3(C_LR_L+C_{GS4}R_{O1})}{1+g_{m2}R_3},$$

$$k_3 = \frac{C_CC_LR_LR_3C_{GS4}R_{O1}}{1+g_{m2}R_3}.$$

In the above, A_{DC} represents the DC gain and ω_Z denotes a zero but this zero is located in the left-half plane which is helpful to improve the phase margin of the system. There are three poles in the system, that is, one dominant real pole (ω_{P1}) and two non-dominant complex poles (ω_{P2}, and ω_{P3}). If we assume that drain resistance of MOSFETs are sufficiently high in a saturated region, the three poles can be approximated as follows.

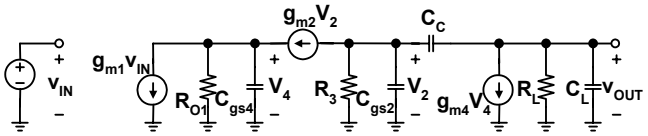

Fig. 2 Small-signal model of the proposed opamp

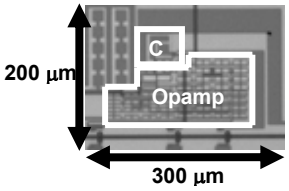

Fig. 3 Chip microphotograph of the proposed opamp

$$\omega_{P1} \approx \frac{1}{R_{O1} g_{m4} R_L C_C} \tag{2}$$

$$\omega_{P2}, \omega_{P3} \approx \frac{g_{m2} C_{GS4}(C_C + C_L) \pm \sqrt{k_4}}{2 C_C C_L C_{GS4}}, \tag{3}$$

where $k_4 = C_{GS4}^2 (C_C + C_L)^2 g_{m2}^2 \quad 4 C_L C_{gs4} g_{m2} g_{m4} C_C^2$.

Eq.(1) and eq.(2) are used to determine gain-bandwidth product of the opamp. To obtain 60 degrees of phase margin, the ω_{P2} and ω_{P3} must be set to at least four times of the ω_{P1} when there is no zero. The ω_{P2} and ω_{P3} are allowed to be lower than two times of the ω_{P1} to obtain the same phase margin because of existence of the ω_Z. Therefore, only small current in the output stage is enough to set the ω_{P2} and ω_{P3} at the required positions. This makes the proposed opamp can achieve lower power consumption than the conventional RC Miller compensated opamp.

The cascode compensation method in [3]-[4] requires current in folded branches which is not exist in the proposed opamp and the compensation approach in [5] performs the same function as the proposed opamp but it requires more current for a common-gate amplifier. Thus, these two approaches always consume higher power than the proposed opamp.

There are more transistors in the active load of the proposed opamp than the conventional opamp in the fig.1. Although these transistors generate noise at the input stage, the noise from these transistors has much less effect than the noise from the input transistors M1 because transconductance of the active load is much smaller than the M1 due to degeneration of the M3.

3. Measurement results

A prototype is manufactured by 0.35μm triple-metal double-poly CMOS process. Fig.3 is a photograph of the tested chip. The open loop frequency response of the manufactured opamp is shown in Fig.4 and Table I. There are a ripple around 50-Hz in the measured results which comes from power-line coupling. Table I shows a performance comparison with the conventional opamp. The proposed phase compensation scheme saves approximately 20% power consumption of the conventional one under the same specifications.

4. Conclusions

This paper proposed a new opamp topology with a source-degenerated phase compensation approach. Since no stacked MOS structures operated in a saturated region are used, it is suitable for low-voltage design. The proposed opamp does not require any extra current consumption to eliminate the feed-forward path in the compensation scheme and there is also no resistor in the proposed topology. Thus, the proposed opamp is suitable for low-power low-cost, and low-voltage applications.

Acknowledgements

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation. Valuable discussion with Dr. H.Ishikuro, Dr. M.Hamada and Dr. T.Furuyama are appreciated. This work is partly supported by Toshiba Corp.

References

[1] D. A. Johns, and K. Martin, *Analog Integrated Circuit Design.* New York: John Wiley & Sons, 1997.

[2] P. R. Gray, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Singapore: John Wiley & Sons, 1997.

[3] D. A. Ribner and M. A. Copeland, IEEE J. Solid-State Circuits, vol. SC-19, No. 6, pp. 919-925, December 1984.

[4] A. Tamtrakarn, and N. Wongkomet, IEEE APCCAS Inter. Conf., pp. 419-424, October 2002.

[5] B. K. Ahuja, IEEE J. Solid-State Circuits, vol. SC-18, No. 6, December 1983.

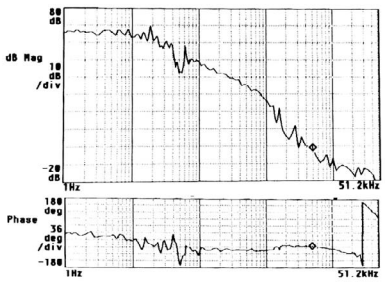

Fig. 4. Measured open-loop frequency response

Table I Measured opamp performance comparison

Specification	Proposed opamp	Conventional RC Miller compensated opamp[a]
ADC	65 dB	85 dB
GBW	5 kHz	5 kHz
Phase margin	68.8 degrees	60 degrees
Input-referred noise @1kHz	$4.3\,\mu V/\sqrt{Hz}$	$4.5\,\mu V/\sqrt{Hz}$
Capacitive load	5 pF	
Supply voltage	3 volts	
Power	1.4 μW	1.8 μW

[a] simulation results