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A Novel Reconfigurable Computing Core for Multimedia System-on-Chip Applications

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1. Introduction

As VLSI technology continues to improve, reconfigurable computing has opened new frontiers in the field of computer architecture. The disadvantage of AISC, less flexible and high cost, is inefficient to use. Our proposed reconfigurable architectuer can achieve both high performance of ASIC and the flexibility. Because reconfigurable hardware can map on different application, we reuse it only by reconfigured. It is obvious to reduce design cost instead of ASIC, needed re-designed a new chip for different applications. And reconfigurable hardware contained flexible function units and re-configured interconnect network. The reconfigurable computing (RC) system combine a reconfigurable hardware with a processor core, and the reconfigurable hardware plays the role as co-processor in the whole system-on-chip. Many kinds of reconfigurable computing architectures are investigated and have published [1]-[7] in the recent decades. We present in this paper a novel RC system, which performs DSP operations efficiently.

In this paper, a novel reconfigurable computing architecture for multimedia SOC applications is proposed. The reconfigurable computing engine is composed of two columns of SIMD based function units, flexible interconnection networks and two-bank on-chip memories. With these components, the reconfigurable computing engine can perform not only 8-bit, 16-bit, 32-bit and 64-bit simple operations but also some novel operations flexibly. Owing to these features, multimedia SOC applications can be performed efficiently on the proposed reconfigurable architecture with high throughput.

2. Reconfigurable Computing Architecture

The reconfigurable computing system consists of an ARM processor, a reconfigurable computing engine, and other peripheral such as direct memory access controller and high bandwidth memory interface. The system controller is a high performance processor, called ARM processor. ARM processor manages the high data-dependent operations. The reconfigurable computing engine is the main component of the reconfigurable computing system. Fig. 1 shows the proposed reconfigurable computing engine. It is composed of function units, data and instruction cache, and high flexible interconnection networks. There are two columns of function units with the SIMD model located in reconfigurable computing engine, and every column has four function units in single slice mode. We can expand this architecture to multiple slices if it is needed. The function units can perform 8 8-bit data operations, 4 16-bit operations, 2 32-bit operations, or a 64-bit operation. The instruction cache and data cache have two banks to take care of two rows of function units. The reconfigurable interconnection network can reallocate and broadcast the data to achieve the flexibility of the communication of the two function units. There are three pipeline stages when processing in the reconfigurable computing engine. The first stage is the instructions fetch/decode and data fetch. The second stage is the execution stage. The third stage is the write-back stage.

Function units are the core of the reconfigurable computing engine. Every function unit consists of ALUs, multipliers, shifters, summation adders, and register files. The function unit can perform 8-bit operations, 16-bit operations, 32-bit operations and 64-bit operations, such as “addition”, “subtraction”, “multiplication”, “comparison”, “data transposition”, and “butterfly-type operation” … etc. Fig. 2 shows reconfigurable function unit in the RC engine. The high performance network between the adjacent function units can optimize the efficiency of resource (function units) allocation and utilization. Thus, we can map lots of algorithms easily in the reconfigurable computing engine.

3. Performance Analysis

Motion estimation is important in video compression. The full-search block-matching algorithm is to calculate the motion vector between the adjacent frames. It takes 4624 cycles to perform the current block-matching process for the proposed reconfigurable computing engine. The literature [4] shows that MorphoSys has the best performance compared with some ASIC architectures and DSP processor, TMS320C64X. However, it takes 4692 cycles to match the current block-matching process for MorphoSys architecture [4]. Among various block transform coding of images and videos, the discrete cosine transform is the most popular and effective one in image and video compression, such as JPEG and MPEG.. For mapping the Chen's algorithm on the proposed reconfigurable computing engine, it takes the proposed reconfigurable computing engine 36 cycles. It takes 37 cycles for MorphoSys [4]. NEC V830R/AV takes 201 cycles [4]. REMARC [5] takes 54 cycles to complete the two dimensional discrete cosine transform. TI TMS320C64x, takes 76 cycles [8]. Intel Pentium II takes

240 cycles. The transform coding in H.264 is modified from discrete cosine transform to integer transform. It only takes the proposed reconfigurable computing engine 8 cycles to execute one macroblock in the fast algorithm for integer transform.

The reconfigurable computing core was implemented using UMC 0.18-μm 1P6M CMOS technology. The core layout of the chip is shown in Fig. 3. It can run up to 100 MHz. The chip features is shown in Table 1. The total gate count is 2.8 million.

4. Conclusions

A novel reconfigurable computing architecture is proposed in this paper. The reconfigurable computing system can perform digital signal processing operations in consumer electronics with high performance and flexibility. With the high flexibility, the reconfigurable computing system can deal with a lot of multimedia applications with high throughput in the future.

References

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Technology	UMC 0.18μm 1P6M
Gate count	2.8 million
layout area	6 x 6 mm^2
Frequency	100Mhz
I/O pads	668
Voltage	1.8V

Table 1. Chip features

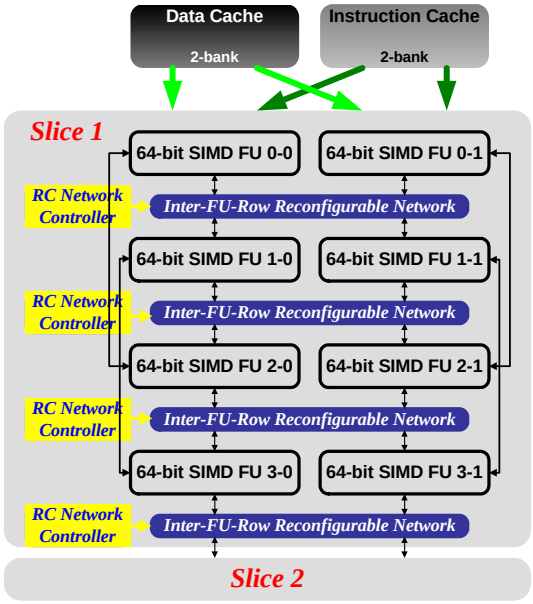

Fig. 1. Diagram of the reconfigurable computing engine

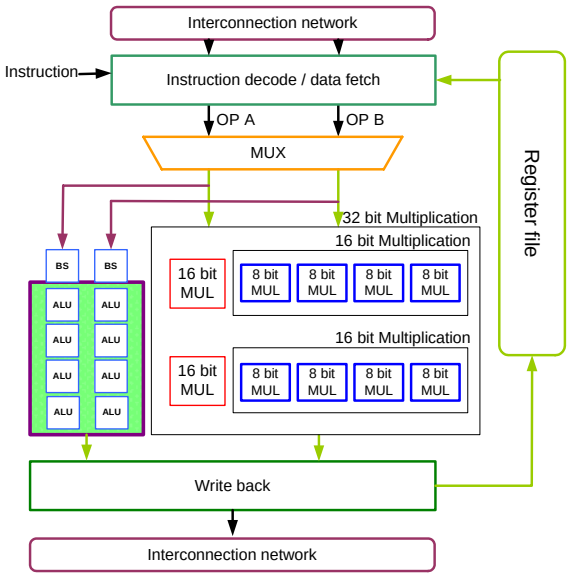

Fig. 2. The reconfigurable function unit

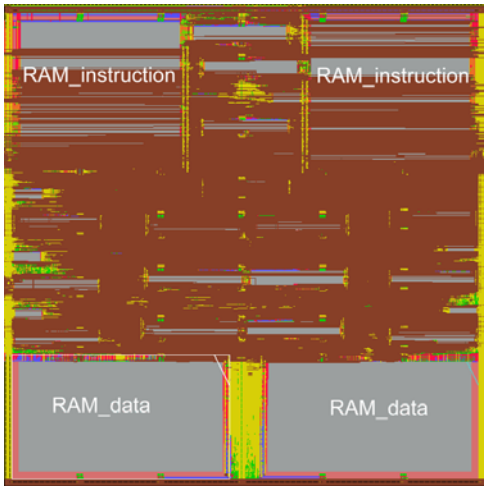

Fig. 3. The core layout of the chip