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An Intelligent Simulation-Based Optimization Technique for Integrated Circuit Design Automation: A Case Study of LNA Circuit Design

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1. Introduction

We present an intelligent simulation-based optimization technique for transistor model parameter extraction and circuit design optimization; in particular, for design of high frequency and analog circuits [1-2]. The prototype of optimization is mainly based on the hybrid intelligent parameter extraction algorithm and SPICE circuit simulation. The developed prototype is tested on several circuits including low noise amplifier (LNA) circuit and show very interesting results. This approach has potential applications to integrated circuit design automation. This CAD technique can be incorporated into electronic computer-aided design (ECAD) software and benefits the communities of design and fabrication.

2. Optimization Methodology

First of all, shown in Fig. 1, the equivalent circuit model of transistors is extracted by using the hybrid intelligent parameter extraction algorithm. The intelligent technique has recently been proposed for nanoscale CMOS and high frequency HBT model parameter extraction in our recent work [3-5]. It mainly includes a data base of empirical extraction rules, numerical optimization algorithm, neural network algorithm, genetic algorithm, and post-verification mechanism. After device base-band model parameter extraction, a set of extracted device model parameters are used to automatically form the SPICE net list for a specified circuit to be optimized. Simulation of the established net list is performed by using the SPICE circuit simulator. The simulation results are evaluated with respect to specified constrains and the specification of electrical characteristics, where the fitness with respect to each iteration process is computed. With the intelligent hybrid optimization technique, evolution on the circuit parameters and allowed design window, such as the device sizes, bias conditions, and temperature, are performed. The obtained newer parameters are used to generate the newer SPICE net list for the next simulation.

3. Results and Discussion

Based on the optimization methodology discussed above, a CAD prototype, shown in Fig. 2, is developed. We have tested on several analog and radio frequency circuits, such as the low noise amplifier, voltage control oscillator, operational amplifier circuits. The inset of Fig. 2 is a pop out window during optimization process. We first perform the parameter optimization on the device model and then the circuit level for the tested LNA circuit, as shown in Fig. 3. There are more than 15 parameters have to be extracted in the designed LNA circuit. As shown in the table I, we partially list the parameters to be optimized in the explored LNA circuit. As shown in Tab. II, there are 7 constraints to be considered in the optimal design of the LNA circuit. The time-domain results are used in the calculation of the corresponding electrical constraints in frequency domain. Each constraint consists of 15 parameters to be optimized. The optimization is subject to minimization of error between the extracted outputs and the specified targets. As shown in Figs. 4, 5, and 6, the optimized S parameters, K factor, the noise figure, and the noise of current are obtained, where the range of frequency is from 2.11GHz to 2.17GHz. As shown in Figs. 4 and 5, the setting of initial values of each circuit element leads to the initial state (dotted lines). After the optimization process, the solid lines show the final optimized results that satisfy the specified targets as shown in Tab. II. Figure 6 shows the optimized noise figure as well as the IIP3 result (it is computed with DFT data). As shown in the table II, we list the final reach specification of the corresponding LNA circuit. We note that the results are automatically obtained without any empirical tuning process. In general, this approach can be applied to other integrated circuit design automation.

4. Conclusions

We have successfully applied the intelligent simulation-based optimization technique to perform circuit design optimization. A LNA circuit with 0.25 and 0.13 μm technologies has been verified. The results show that this approach is accurate and computationally efficient. We believe that this approach will benefit the design community; in particular, for radio and analog circuit design optimization.

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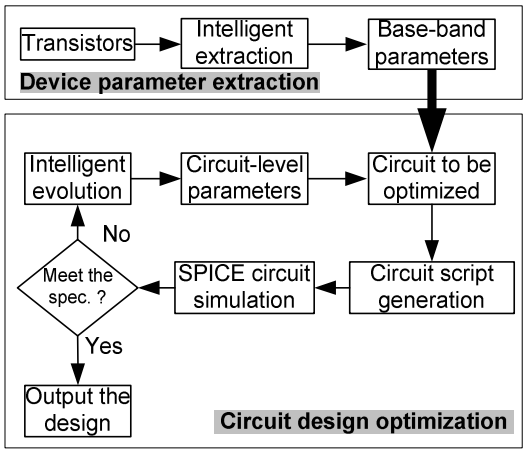

Figure1. An architecture of the proposed optimization methodology for general circuit design automation.

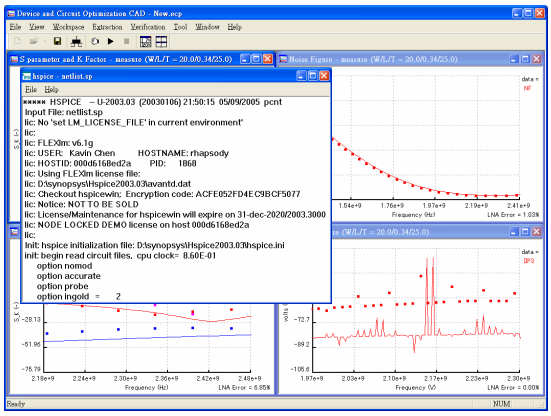

Figure 2. An illustration of the user interface of the developed optimization CAD prototype.

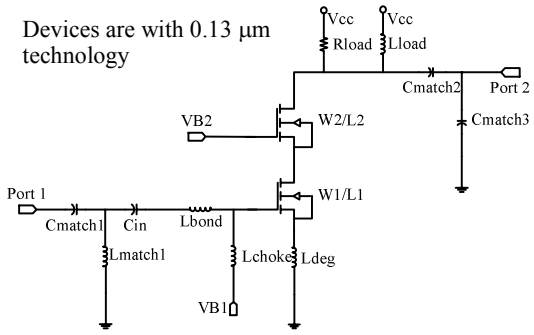

Figure 3. A low noise amplifier (LNA) circuit. There are more than 15 parameters to be optimized.

Table I. A list of the LNA circuit parameters, unit, ranges, and optimal extracted values.

Parameter	Unit	Range	Extracted value
Cmatch1	F	500 ~ 700	657.738f
Cmatch2	F	1~10	5.05p
Cmatch3	F	1~10	4.551p
Lbond	H	0~3	1.058n
Ldeg	H	0~3	0.985n
Lmatch1	H	1~10	5.257n

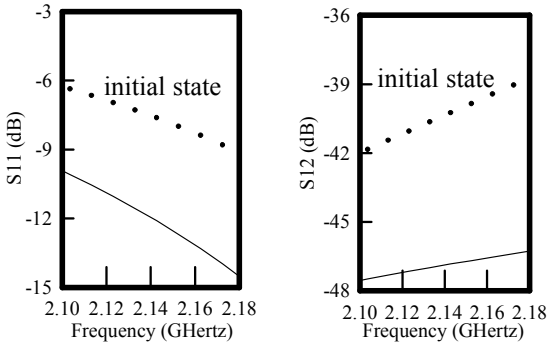

Figure 4. The optimized (solid lines) S11 and S12.

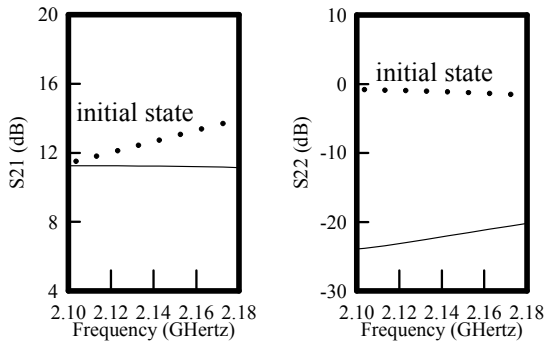

Figure 5. The optimized (solid lines) S21 and S22.

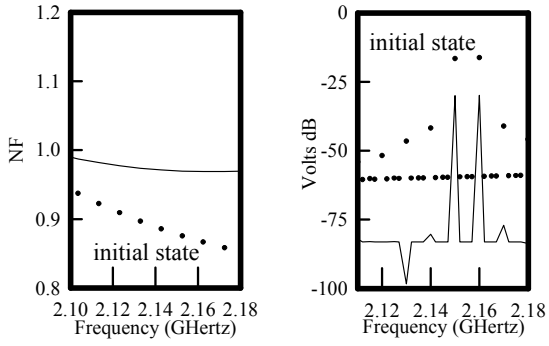

Figure 6. The optimized results (solid lines) of the noise figure and DFT. The original IIP3 is –12.575, and the optimized IIP3 is -2.75.

Table II. The specification of the designed LNA operated in the range of 2.11~2.17GHz and the final extracted results.

Output Specification	Wanted Target	Extracted Result
S11	< -10dB	-15dB
S22	< -10dB	-25dB
S12	< -25dB	-40dB
S21	> 10dB	13dB
K factor	> 1	10
Noise figure	< 2	0.9
IIP3	> -10	-2.75