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A Novel Fast Lock-in PLL Frequency Synthesizer with Direct Frequency Presetting Circuit

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1. Introduction

One of the challenges in modern wireless communications is the development of fast lock-in phase-locked loop (PLL) frequency synthesizers. In order to realize the fast lock-in PLL synthesizer, dynamic loop bandwidth method was proposed [1]. However, the loop bandwidth is limited by channel spacing. Recently fractional-N PLL synthesizer was proposed [2]. The kind of the synthesizer can speed up the lock-in process by increasing the reference frequency and the loop bandwidth. But it brings additional fractional spurs that are hard to be removed.

This paper proposes a novel fast lock-in PLL frequency synthesizer. The synthesizer includes a novel VCO with direct frequency presetting. The frequency presetting technique can speed up the lock-in process remarkably and avoid the tradeoff between the lock-in speed and the phase noise/spurs. The novel synthesizer can automatically compensate the frequency variation with temperature.

2. A novel frequency synthesizer

Figure 1 shows the block diagram of the proposed novel fast lock-in PLL synthesizer. The digital controller not only outputs the divide ratio N but also directly presets the oscillation frequency of the VCO with a frequency-presetting digital signal C.

Figure 2 shows the novel mixed-signal-controlled VCO with frequency presetting mechanism. The frequency-presetting signal C presets the output frequency of the novel VCO with small initial frequency error. Then the output signal V_a of the loop filter precisely tunes the frequency of VCO. The VCO circuit can automatically compensate the frequency variation with temperature. V_p signal is used to compensate the frequency variation originating from the fabrication error.

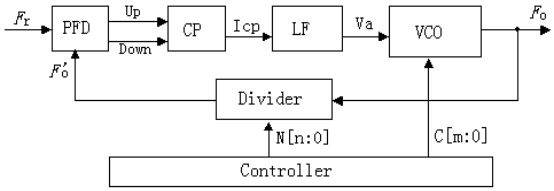

Figure 1. Novel frequency presetting PLL synthesizer

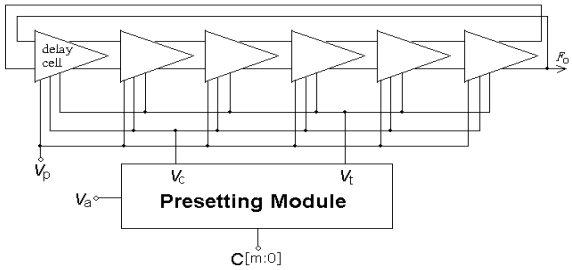

Figure 2. the novel mixed-signal VCO

Figure 3 shows the proposed delay cell circuit in the novel VCO. It is a full-swing differential inverter with parallel active loads of PMOS transistors. M3 and M4 transistors are controlled by output V_c of the presetting module to tune the frequency of VCO. M5 and M6 transistors are used to compensate the variation in the delay time due to the fabrication error. M7 and M8 transistors are used to compensate the variation in the delay time due to temperature effect.

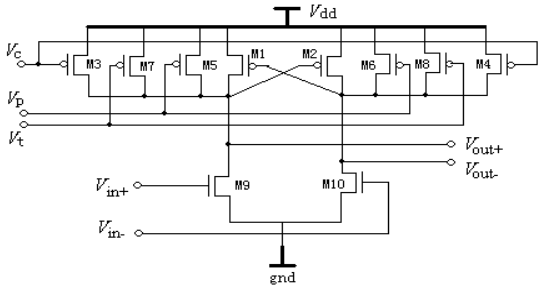

Figure 3. Delay cell in the novel VCO

The circuit of the presetting module is shown in Figure 4. Because there is a nonlinear relation between the frequency presetting signal C and the oscillation frequency of VCO, we design an additional current compensation network to reduce the presetting frequency error within +/-1MHz and to shorten the lock-in time of the frequency

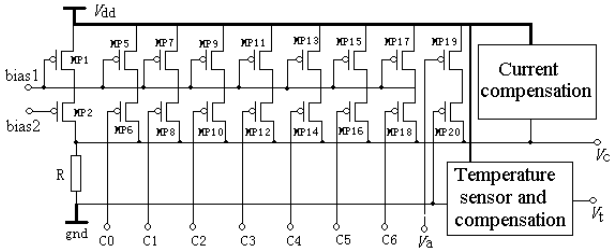

Figure 4. The mixed-signal presetting module

synthesizer. We found the VCO frequency varies with temperature about 1.4MHz/^{0}C. We designed temperature sensor and compensation circuit.

3. Simulation and Results

The novel fast lock-in PLL synthesizer was designed basing on a 0.35um CMOS Process. The layout of the synthesizer is shown in Figure 5. The capacitors of loop filter are on chip. The whole chip area is about 0.4 mm^2. The post simulation of the synthesizer was carried out. In order to compare the novel synthesizer with the conventional one, we also designed a conventional synthesizer with similar circuit parameters. The gain Kv of the novel VCO is 20MHz/V that is much smaller than the gain 200 MHz/V of the conventional VCO.

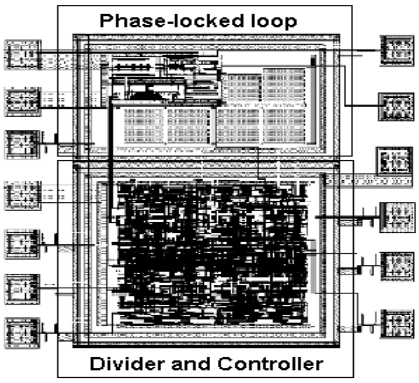

Figure 5 Layout of proposed synthesizer

Figure 6 shows the frequency hopping characteristics of the proposed and conventional synthesizers. We started up the synthesizers and changed the divide ratio N to make the frequency hopping from 1GHz to 935MHz at 62us. The output signal V_a of the loop filter in the novel synthesizer convergences within a small error of +/-1.5mV in 2us. It means that the synthesizer has locked in within frequency tolerance of 30KHz in 2us after the divide ratio N was changed. However, the lock-in time of the conventional synthesizer is more than 37us when frequency tolerance is within 200KHz.

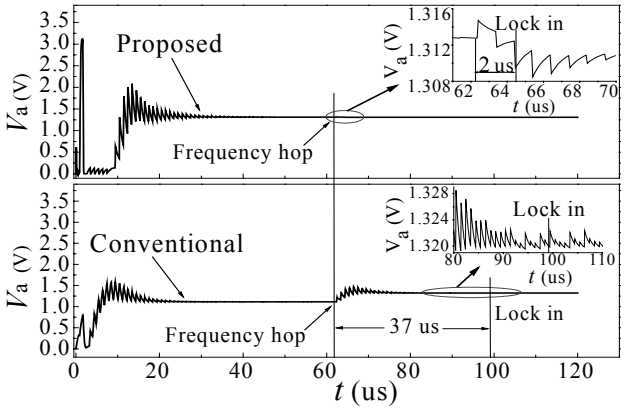

Figure 6. The frequency hopping characteristics of the proposed and conventional synthesizers

The design parameters and simulation results are summarized in table I. The results demonstrate that the frequency presetting method is much effective and can speed up the lock-in process of the synthesizer remarkably. The novel synthesizer can avoid the tradeoff between the lock-in speed and the phase noise/spurs. The chip area of the proposed synthesizer is much smaller than that of the conventional synthesizer.

Table I. Design parameters and performance of proposed and conventional synthesizers

	Proposed synthesizer	Conventional synthesizer
Output frequency range	1140MHz ~840MHz	1160MHz ~820MHz
Reference frequency	1MHz	1MHz
Loop bandwidth	67KHz	67KHz
Phase margin	53^0	53^0
Charge pump current	200uA	200uA
VCO gain	20MHz/V	200MHz/V
Lock-in Frequency tolerance	30KHz	200KHz
Lock-in time	2us	37us
VCO phase noise (Fo = 900MHz)	-104dBc/Hz @1MHz	-105dBc/Hz @1MHz
Capacitors of LF	On chip	Not on chip

4. Conclusions

This paper proposed a novel fast lock-in PLL frequency synthesizer. We designed the circuits basing on a 0.35um CMOS process and carried out the post simulation. The results demonstrate that the novel synthesizer can speed up the lock-in process much and lock in within 30 KHz frequency tolerance in 2us. The novel synthesizer avoids the tradeoff between the lock-in speed and the phase noise/spurs. The capacitors in the loop filter were smaller and can be integrated on chip.

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