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P5-5

Estimation of Wire Length Distribution for Evaluating Performance Improvement of Three-Dimensional LSI

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1. Introduction

The demand for higher wiring connectivity within a chip has become strong as the transistor count of system-on-a chip (SoC) increases. In order to increase the wiring connectivity and to achieve higher LSI performance, we have developed a three-dimensional (3D) integration technology using a wafer bonding technique [1]-[3]. Several LSI wafers are vertically stacked to fabricate 3D LSI as shown in Fig. 1. More than 10^5 vertical interconnections per chip are formed in the 3D LSI. Thus, the wiring connectivity can be increased while the number of long wiring such as global wiring is reduced. This results in the dramatic reduction of total wiring length and it leads to a reduction of parasitic capacitance and resistance. As a result, the signal-propagation delay and the system power consumption are significantly reduced.

In this paper, wire length distribution of the 3D LSI is estimated by developing a simulated quenching program for 3D placement of standard cells in order to quantitatively evaluate the performance improvement of 3D LSI.

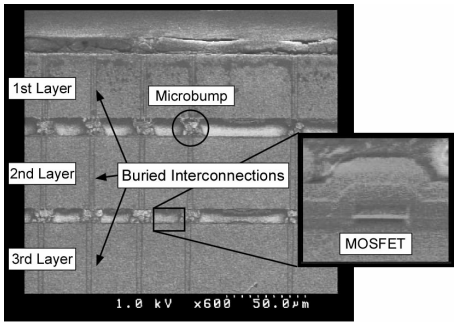


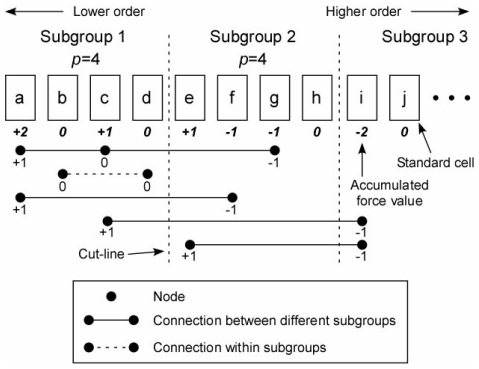
Fig. 1. SEM cross-sectional image of 3D LSI with three layers.

2. Simulated Quenching for 3D LSI

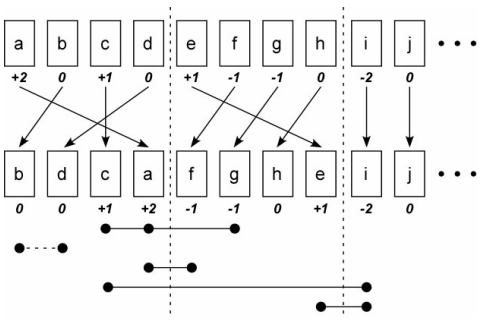
The standard cell placement is a NP-complete combinational optimization problem. Therefore, it is very difficult to calculate total wire lengths for whole placement patterns. In this work, a simulated quenching is adopted to obtain a quasi-optimum solution for the 3D placement of the standard cells because of its higher speed compared to other methods such as simulated annealing [4], [5].

Figure 2 shows an example of linear placement sequence with ten standard cells using simulated quenching. The standard cells are classified into some subgroups by placing cut-lines with a constant pitch (= p) on the current linear placement. Force values are provided for the standard cells which have nodes connected with other standard cells. If a standard cell is located at the lowest order of connection with other standard cells located in different subgroups, the force value of the standard cell is increased by one. On the other hand, if a standard cell is located at the highest order of connection with other standard cells located in different subgroups, the force value of the standard cell is decreased by one. The standard cells are sorted within each subgroup according to the accumulated force values of the standard cells. If a standard cell has the larger positive force value, this standard cell is replaced toward the higher order within the subgroup. The standard cells are repeatedly sorted within the subgroups for each pitch value p which is gradually decreased from sufficiently large value to two as follows.

$$p = p - 0.03 \times \frac{p}{\log_2 p} \tag{1}$$



(a) Subgroup generation and force value accumulation.



(b) Sorting within subgroups.

Fig. 2. Linear placement sequence using simulated quenching.

The 3D placement of standard cells can be developed based on this linear placement using simulated quenching. Cut-lines with pitch value p are placed along three axes (X, Y, Z) after the initial 3D placement of standard cells. A subgroup is defined as an area enclosed by the cut-lines placed along three axes as shown in Fig. 3. Within each

subgroup, the standard cells are sorted in order of X, Y and Z as with the linear sorting. Then, the standard cells are three-dimensionally sorted within the subgroups for each pitch value *p*. Finally, a quasi-optimum solution to reduce a maximum wire length and a total wire length can be achieved.

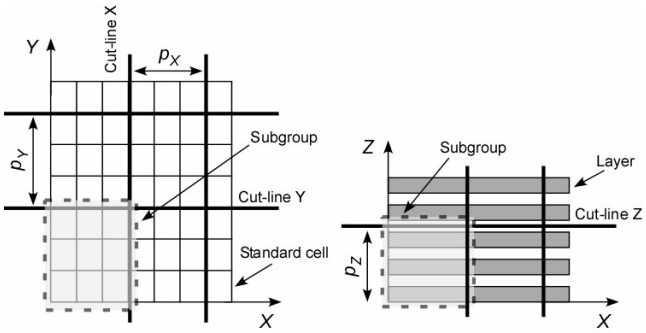


Fig. 3. Simulated quenching for placing 3D placement.

3. Wire Length Distribution of 3D LSI

We have developed a program for 3D placement using the simulated quenching in order to estimate a wire length distribution of 3D LSI comparing it to that of conventional two-dimensional LSI. The IBM-PLACE benchmark circuit was used for the estimation of a wire length distribution. The minimum unit cell size is defined as one in direction X and five in direction Y based on the size of an inverter cell. The length Z of vertical interconnection is set as 15 based on previously fabricated vertical interconnection. The wire length is defined as a Manhattan distance as shown in Fig. 4.

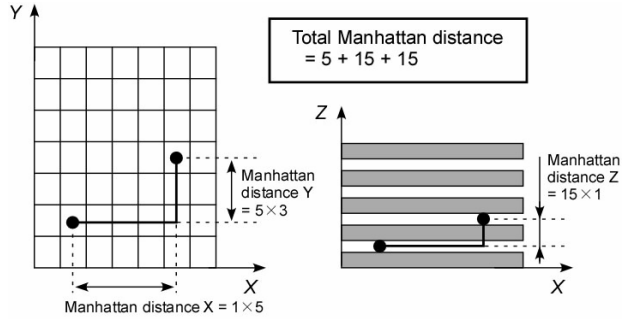


Fig. 4. Manhattan distance within 3D LSI.

In the simulation using the 3D placement program, one of IBM-PLACE benchmark circuits, ibm01, was used [6]. Figure 5 shows the simulation results of calculating wire length distribution with several chip layers. With the increase of the chip layers, the number of shorter wirings increased while the number of longer wirings decreased. Figures 6 and 7 show the simulation results of calculating a total wire length and a maximum wire length with several chip layers. The total wire length is reduced by around 27% in the three layer placement compared to the conventional one-layer placement. The maximum wire length in the three layer placement is also reduced by around 36% compared to the conventional one-layer placement. Therefore, parasitic capacitance and resistance can be reduced by using 3D LSI. Consequently, the signal-propagation delay and the system power consumption can be reduced.

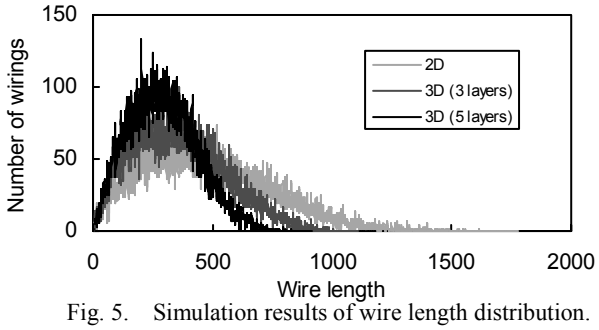


Fig. 5. Simulation results of wire length distribution.

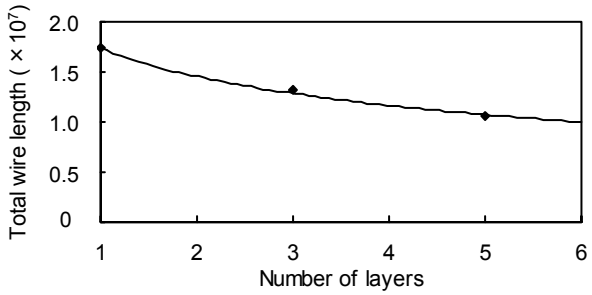


Fig. 6. Simulation results of total wire length.

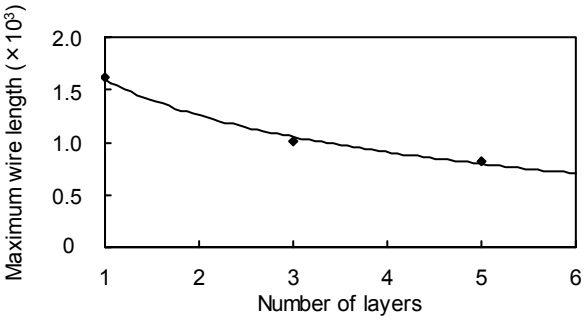


Fig. 7. Simulation results of maximum wire length.

4. Conclusion

In order to evaluate the performance improvement of the 3D LSI, a wire length distribution in 3D LSI was estimated by developing a simulation program for 3D placement of standard cells. The total wire length and the maximum wire length were reduced by around 27% and 36% respectively in the three layer placement compared to those of the conventional one-layer placement when IBM-PLACE benchmark circuit was used. Thus, we prospected that the parasitic capacitance and resistance can be reduced by using 3D LSI and hence the signal-propagation delay and the system power consumption can be reduced.

References

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