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No Feedback ΔΣ ADC for High Frequency Operation Using Frequency ΔΣ Modulator

W. Matsubara, M. Sakou, K. Maezawa, and T. Mizutani

Graduate School of Engineering, Nagoya University
Furo-cho, Chikusa-ku, Nagoya-shi, 464-8603 Japan
w_matuba@echo.nuee.nagoya-u.ac.jp

1. Introduction

Oversampling A/D converters using ΔΣ modulation are used for various applications since they have a significant advantage compared to other types of ADCs; higher resolution can be easily obtained by increasing the sampling rate. They do not require high-accuracy analog components and are suitable for VLSI implementation. However, the sampling rate and hence the resolution of ΔΣ ADCs are restricted by the operation speed of the negative feedback loop. To overcome this limitation, this paper discusses a ΔΣ ADC having no feedback loop and its implementation.

2. Frequency Delta-Sigma Modulator

Figure 1 shows the block diagram of the ΔΣ ADC. The input analog signal is first converted to the pulse density modulation signal, and then it is converted to the Nyquist rate high-resolution (multi-bit) digital signal by a decimation filter. The key component of this is the ΔΣ modulator (DSM), which converts the analog signal to the pulse density digital signal. Here, we employ a novel ΔΣ modulation technique using a VCO [1, 2]. This DSM will be referred to as a frequency DSM (FDSM). The Configuration of the FDSM is shown in Fig. 2 together with the conventional one. This implementation is based on the fact that the phase of the frequency modulation (FM) signal from VCO, θ(t), is the integral of the input signal $x(\tau)$ as

$$\theta(t) = 2\pi\int_{-\infty}^{t} (f_C + kx(\tau))d\tau$$

Here, f_c represents the output frequency of the VCO (carrier frequency) when input is zero, and k the frequency sensitivity. Therefore, the integrator in the conventional configuration can be removed. Moreover, the negative feedback is inherently embedded in the VCO, because the phase returns to zero when it reaches 2π. Owing to these features the feedback loop can be also removed. Using the 1-bit quantizer and the XOR the ideal pulse density signal can be obtained. This implementation has a significant advantage in that there is no feedback loop and no D/A converter, which limit the operation speed of the DSM. However, this has a difficult problem in practical use; the VCO must have high linearity and wide range of frequency modulation. Due to this problem this technique has never been widely used for ADCs.

3. The Novel VCO Having Wide Modulation Range and High Linearity

Here, we propose a novel circuit to make wide range VCO with high linearity suitable for FDSM. The block diagram is shown in Fig. 3. It consists of two VCOs, a mixier, and a low pass filter (LPF). Complementary signals with different dc biases are fed to the two VCOs. Their output FM signals are converted to the difference frequency using the mixer and the LPF. With this configuration, the frequency modulation ratio to the carrier frequency can be much reduced for the individual VCOs. This should also improve the linearity. For example, a VCO operated at 10GHz f_c with ±250MHz modulation, and the other one operated at 9.5GHz f_c with ±250MHz modulation produces 500 MHz f_c ±500 MHz modulation. Moreover, this has another advantage; the bias line and substrate noises, which are significant noise sources in mixed signal circuits like ADC, can be canceled.

We designed and simulated this circuit to verify the concept using 0.35-μm CMOS devices. For simplicity, CML ring oscillators were used for the individual VCOs. The frequencies are controlled by the gate bias to the current sources. The result of the wide range FM signal generation is shown in Fig. 4. One VCO was operated at 1.62GHz f_c with ± 50MHz modulation, and the other was operated at 1.72GHz f_c with ±50MHz modulation. As a result, we obtained FM signal with 100MHz f_c with ±100MHz modulation. For comparison, the result of the conventional VCO using one ring oscillator is shown in Fig. 5. It is clearly shown that the linearity is much improved. Finally, we designed and simulated the DSM using above circuit. Figure 6 shows the noise spectrum of the FDSM. Good noise shaping with relatively small harmonics can be obtained. This indicates the promise of the proposed circuit for wide band, high resolution ADCs.

References

[1] M. Hovin, et al., IEEE J. Solid-State Circ., 32, (1997) 13.

[2] A. Iwata, et al., IEEE Trans. Circ. Syst. II, 46, 941, 1999.

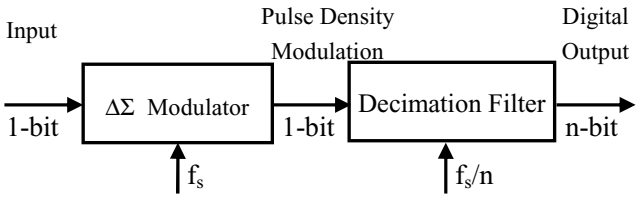

Fig. 1 Block diagram of ΔΣ ADCs.

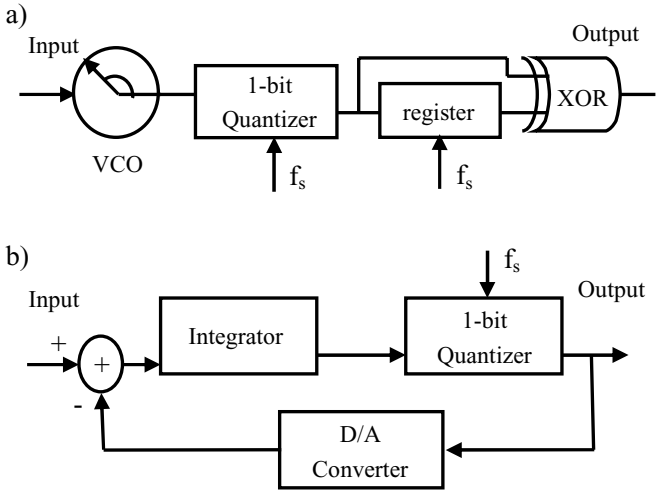

Fig. 2 Block diagram of ΔΣ modulators.
a) Frequency ΔΣ modulator using a VCO.
b) Conventional ΔΣ modulator.

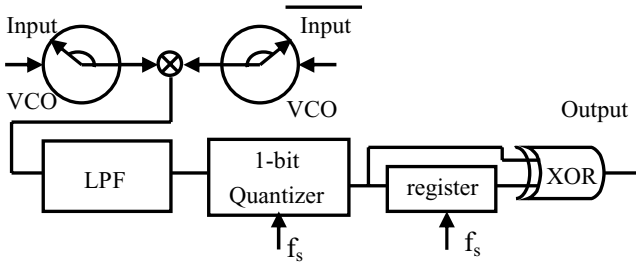

Fig. 3 Frequency ΔΣ modulator using the novel VCO.

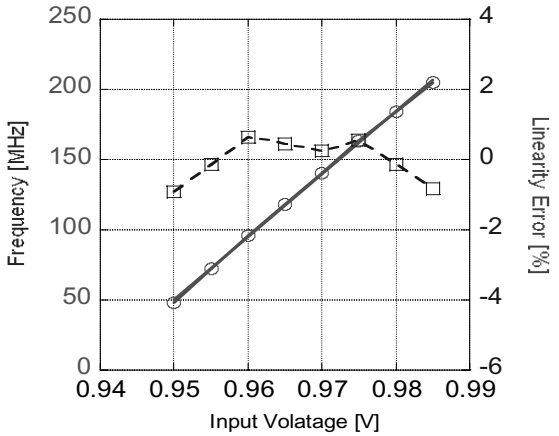

Fig. 4 Output frequency and its linearity error of the novel VCO obtained from HSPICE simulation.

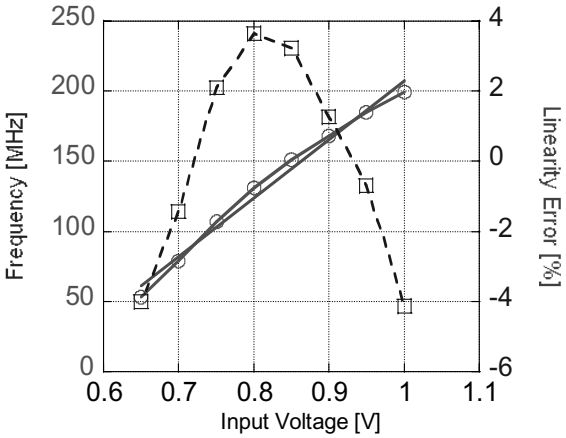

Fig. 5 Output frequency and its linearity error of the conventional VCO obtained from HSPICE simulation.

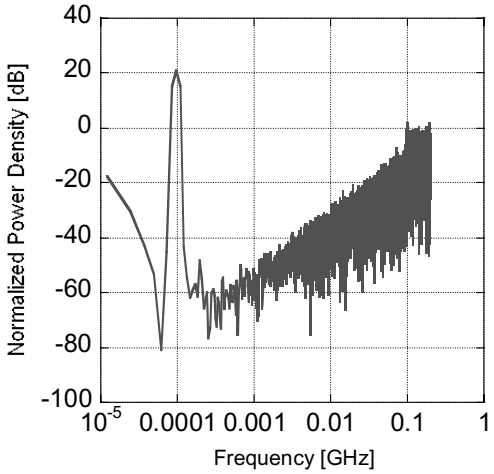

Fig. 6 Obtained output spectrum of the ΔΣ modulator using the novel VCO. The input signal was 100kHz, and the FM signal was 100MHz with maximum modulation of 50MHz.