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P5-8 A Novel Operation Scheme for Realizing Combined Linear-Logarithmic Response in Photodiode-Type Active Pixel Sensor Cells

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A novel operation scheme that realizes combined linear-logarithmic response in conventional photodiode-type active pixel sensor (APS) cells is presented. It has been revealed that, by setting the reset transistor in weak inversion through properly selected bias voltages, conventional photodiode-type APS cells can be operated with seamlessly combined linear-logarithmic response. Modification to the conventional APS cells that enhances their dynamic ranges in linear response mode is also described.

Introduction

CMOS active pixel sensors (APSs) are now widely used for portable, low-voltage applications such as wireless handy telephones where power consumption is the major concern [1]. Conventionally APSs that have linear response to the incident light intensity have been used. Figure 1(a) shows the circuit diagram of one type of such linear APS cells (namely, photodiode-type (PD) APS cell). After charging up its diffusion capacitance (C_{PD}) through the reset MOSFET M1, the photodiode is exposed to incident light. The generated photocurrent discharges the diffusion capacitance and decreases V_{PD}. This decrease in V_{PD} (ΔV_{PD}) is read by a source follower amplifier M2 followed by a data selector M3, ΔV_{PD} being converterd to I_{SIG} (see the timing chart shown in Fig.1(b)).

One of the drawbacks of CMOS APSs with linear response is their considerably narrow dynamic range (two or three orders of magnitude) [2], thus I_{SIG} is easily saturated as light intensity increases (see Fig.1(b)). Logarithmic transformation [1] is one solution to a wider dynamic range, and the authors have proposed an APS cell with selectable linear/logarithmic response [3]. Although it realizes two distinct operation modes with either linear or logarithmic response [3], it is not possible to directly combine two images taken in both response modes because output signal current indeed differs in each mode.

In this paper the authors newly propose an operation scheme which realizes seamlessly combined linear-logarithmic response in PD APS cells. Circuit simulation by SPICE 3f5 with the BSIM3v3.1 MOSFET model (Fig.2) has revealed that, by proper selection of bias voltages, conventional PD APS cells can achieve such combined response, thus widening their dynamic ranges. Although Hara *et al.* [4] has recently reported a linear-logarithmic CMOS PD APS cell with one additional MOSFET (*i.e.*, their cell has four MOSFETs), the authors believe that the operating scheme described in this paper is more suitable especially for cost-conscious applications. Modification that enhances dynamic ranges of APSs in linear response mode is also described.

Basic Concepts

Figure 3 illustrates the proposed operation scheme for PD APS cells. The major difference between the conventional and the proposed scheme is that, after charging up C_{PD}, the voltage applied to the gate of M1 stays at V_M, an intermediate value between V_{DD} and *Gnd* (= 0 V), rather than returns to 0 V. In the case where the light intensity is not strong enough to discharge C_{PD} to cause V_{PD} to be lower than $V(V_M)$, which is a function of V_M, ΔV_{PD} is proportional to the light intensity as in the conventional operation mode. In the case where the light intensity is strong enough to make V_{PD} below $V(V_M)$, because M1 becomes biased in weak inversion, finite amount of current flows through M1, which balances with the photo-generated current in the photodiode as in PD APS cells with logarithmic response [1]. In this situation ΔV_{PD} does not saturate easily compared with the case of linear operation mode shown in Fig.1(b).

Simulated Results

All of the circuit simulation results were obtained using the same MOSFET model whose current-voltage characteristics is shown in Fig.2. M1, M2 and M3 were assumed to be identical and to be placed in the same p-well region connected to *Gnd*.

The relationship between photo-generated current and signal current shown in both Figs.4 and 5 clearly indicates that the proposed operation scheme enables the conventional PD APS cells to have seamlessly-combined linear-logarithmic response. They also illustrate the V_M dependence, *i.e.*, the crossover point which combines linear and logarithmic response depends on the value of V_M.

Our results shown in Fig.6 suggests that, if M1, M2 and M3 has the individual body terminals which are separated electrically from each other and are connected to the respective source terminal, ΔI_{SIG} in linear response mode can be by 50 % enhanced as compared with the case where all MOSFETs are placed in the same well. This is due to the elimination of V_{TH} increase by the so-called "substrate bias" effect.

Acknowledgement

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References

[1] E.R.Fossum, IEEE Trans. Electron. Devices, **44** (1997) 1689.
[2] S.G.Chamberlain, IEEE J. Solid-State Circuits, **SC-4** (1969) 333.
[3] M.Terauchi, A.Hamasaki and A.Suketa, Jap. J. Appl. Phys, **44** (2005) 2347.
[4] K.Hara, H.Kubo, M.Kimura, F.Murao and S.Komori, Tech. Dig. of ISSCC2005, p.354.

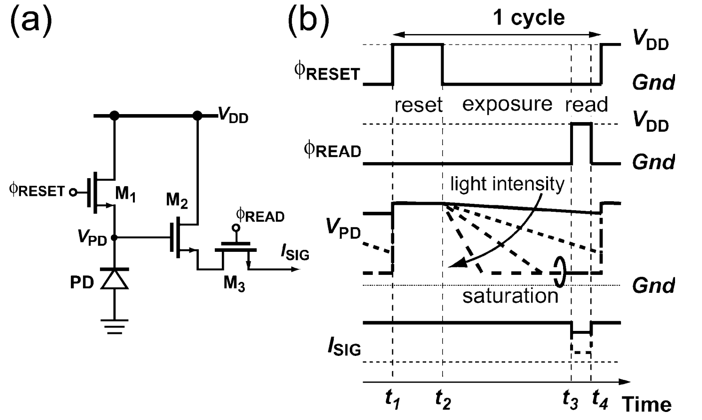

Fig.1(a) Circuit diagram of conventional PD APS cells. (b) Timing chart of conventional operation scheme for PD APS cells shown in Fig.1(a).

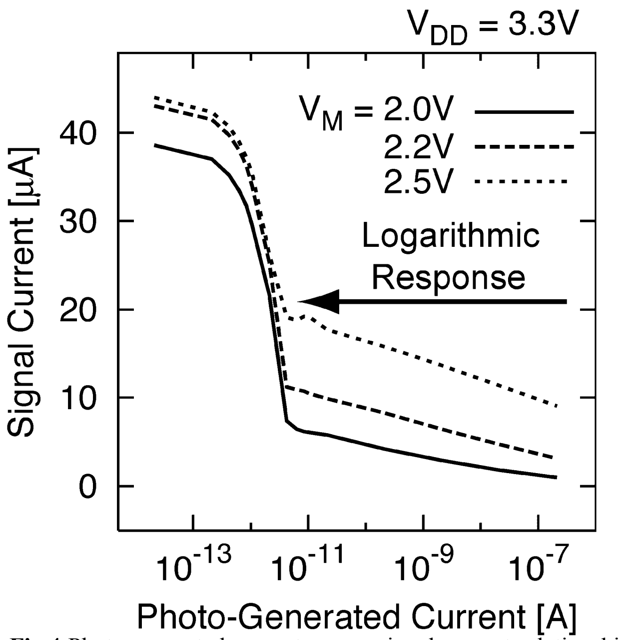

Fig.4 Photo-generated current versus signal current relationship. This clearly illustrates the combined linear-logarithmic response.

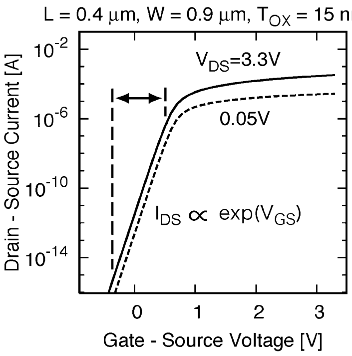

Fig.2 Simulated subthreshold characteristics of an MOSFET by SPICE 3f5 with the BSIM3v3.1 MOSFET model.

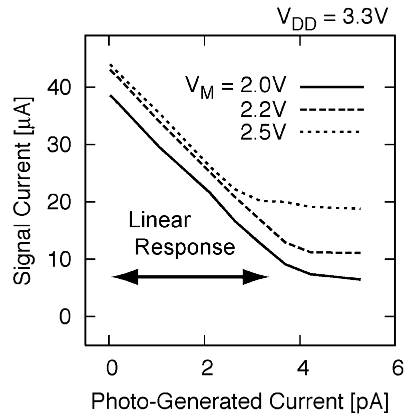

Fig.5 Photo-generated current versus signal current relationship in linear response region.

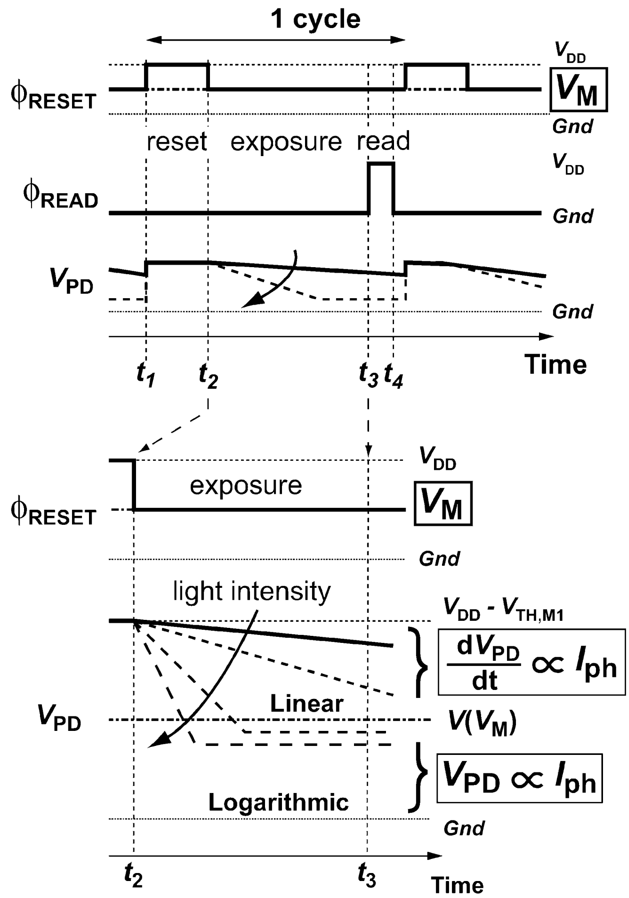

Fig.3 Timing chart of the proposed operation scheme for PD APS cells. After charging up C_{PD}, the voltage applied to the gate of M1 stays at V_M, an intermediate value between V_{DD} and *Gnd*, and never returns to *Gnd*.

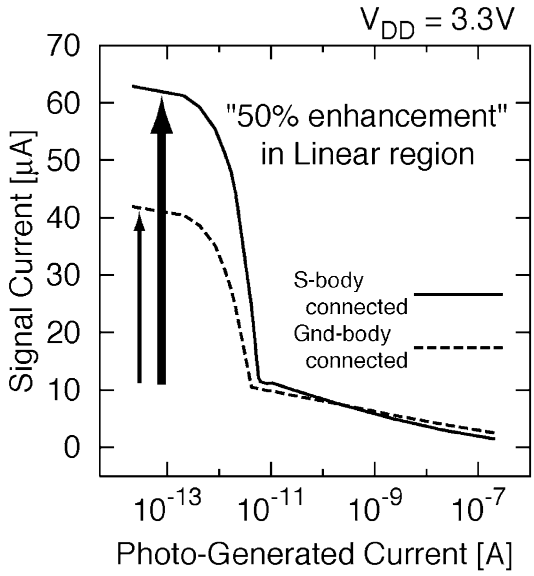

Fig.6 The relationship between photo-generated current and signal current where M1, M2 and M3 has the individual body terminal separated electrically from each other and connected to the respective source terminal. ΔI_{SIG} can be by 50% enhanced as compared with the case where M1, M2 and M3 has common body connected to *Gnd*.