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P5-9

New TxID sequence and Matched Filter implementation for ATSC DTV

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1. Introduction

Recently, new proposals and studies [1][2] for TxID (Transmitter Identification) technology of ATSC (Advanced Television Systems Committee) standard are vigorously progressing, that is a core technique to implement terrestrial DTV (Digital Television) system based on advanced SFN (Signal Frequency Network). In TxID techniques, a very long SF (Spreading Factor) of 64896 chips is used for watermarking in each field and individual unique TxID sequence is assigned for each OCR (On Channel Repeater) as shown in Fig. 1. Therefore, it is very important to select an efficient spreading-code set with good correlation property for realizing efficient TxID, and also it's more important to find an efficient hardware implantation of MF (Matched Filter) with long SF of 64896 chips. However, conventional TxID techniques [3][4] based on the Kasami sequences cause truncated error and ICI (Inter Code Interference). Furthermore, conventional TxID techniques [1]-[4] have no any consideration about efficient MF hardware implementation techniques [5]. Hence, in this paper, we propose a new TxID sequence without any ICI and truncation error. Moreover, we design a new TxID sequence based efficient MF architecture with new partial correlation structure. Using simulation result and digital hardware implementation with FPGA (Field Programmable Gate Array), we will certify the availability and superiority of proposed algorithms.

2. Efficient MF architecture for DTV TxID using new TxID sequences

New TxID sequences without Truncation error and ICI

In this paper, we propose a new TxID sequence by improvement of ZCD sequences [6][7] as shown eq. (1).

$$\begin{aligned} C_N = \{ & ABZ_i\ A\text{-}BZ_i\ ABZ_i\ \text{-}ABZ_i\ ABZ_i\ A\text{-}BZ_i\ \text{-}A\text{-}BZ_i\ A\text{-}BZ_i \\ & ABZ_i\ A\text{-}BZ_i\ ABZ_i\ \text{-}ABZ_i\ \text{-}A\text{-}BZ_i\ \text{-}ABZ_i\ ABZ_i\ \text{-}ABZ_i \\ & ABZ_i\ A\text{-}BZ_i\ ABZ_i\ \text{-}ABZ_i\ ABZ_i\ A\text{-}BZ_i\ \text{-}A\text{-}BZ_i\ A\text{-}BZ_i \\ & \text{-}A\text{-}BZ_i\ \text{-}ABZ_i\ \text{-}A\text{-}BZ_i\ A\text{-}BZ_i\ ABZ_i\ A\text{-}BZ_i\ \text{-}A\text{-}BZ_i\ A\text{-}BZ_i\} \end{aligned} \quad (1)$$

Where, A and B are Binary ZCD sequences. And i and Z_i means the number of inserted zeros and zero ICI duration with $(0.75N \times i+1)$ chips, respectively. In the general TxID schemes, TxID sequence with N= 64896chips and Z_i of 1004 zeros can be used. Moreover, since sequence length corresponds to the watermarking length, truncation error of the proposed sequences does not exist.

Efficient MF architecture for DTV TxID

In this paper, we consider and design an efficient MF architecture based on the new ZCD code controller method and new partial correlation structure which decrease the total correlation computation related to zero coefficients as showing in Fig. 2. The structure of proposed MF divided into 1-order block and 2-order block as showing in Fig. 3. The 1-order block of the proposed MF which is newly implemented in this section consist of 1024 4-chip delay elements, 592 inverters, two adder blocks to compute A and B as shown in eq. (1). And 2-order block is implemented by 11 adders, 5 inverters, 5 delay elements which consist of m shift registers connected to 1-order block. Here, m={1024, 2048, 4096, 8192, 16384}.

3. Implementation and verification of proposed MF

In this section, we estimated proposed MF architecture using MATLAB simulation and implemented it using Virtex-Ⅱ Xilinx FPGA. Table I shows the comparison results of proposed filter with general FIFO (First Input First Out) type MF [8]. Here, in the case of proposed MF, register numbers are similar to existing FIFO type MF, but the number of adder is 127,734(98.42%), and its number is remarkably smaller than FIFO type MF. The reason is pipeline registers are decreased relatively because Proposed MF always computes correlation values using only two states and ZCD code controller. In this paper, we verified the MF performance through the transceiver signal of DAC (digital-to-analog converter) and ADC (analog-to-digital converter) and implemented digital hardware using Virtex-Ⅱ(XC2V3000) Xilinx FPGA. Also we measured the correlation-output of implemented MF using Tektronix digital oscilloscope (TDS8200). Fig. 4 shows ACF (auto correlation function) peak of Matlab simulation, and Fig. 5 shows a measured MF output. From the comparison of Fig. 4 and Fig. 5, we certified the implementation ability and operational performance of proposed MF.

4. Conclusions

In this paper, we proposed new TxID sequence and Matched Filter implementation for ATSC DTV. Newly proposed TxID sequences have no any ICI and trunca-

tion error. Moreover, new TxID sequence based efficient MF architecture with new partial correlation structure is design and proposed. Using simulation result and digital hardware implementation with FPGA (Field Programmable Gate Array), we certified the availability and superiority of proposed algorithms.

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Table I. MF performance comparison

MF type	14bits Register number	14bits Adder number	Power consumption.
Conventional FIFO type MF [8]	64,896	129,791	269.956mW
Proposed MF	64,512	2,057	87.296mW

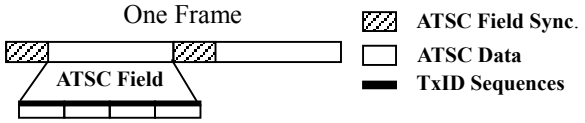

Fig. 1 Watermarking principle for TxID of ATSC-DTV [2]-[4]

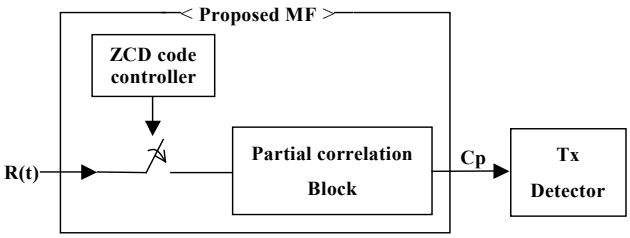

Fig. 2 Proposed MF Block for TxID of ATSC-DTV

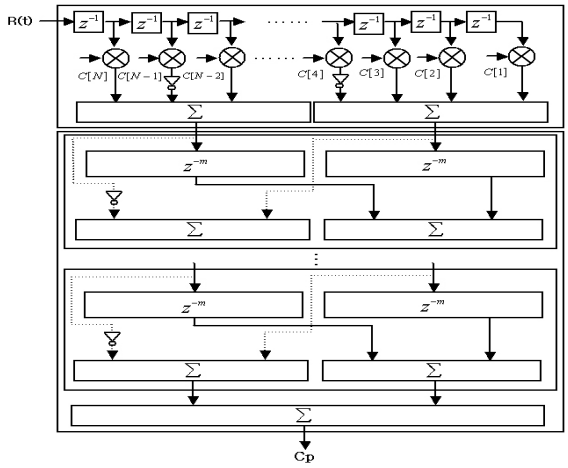

Fig. 3 New partial correlation architecture of proposed TxID MF

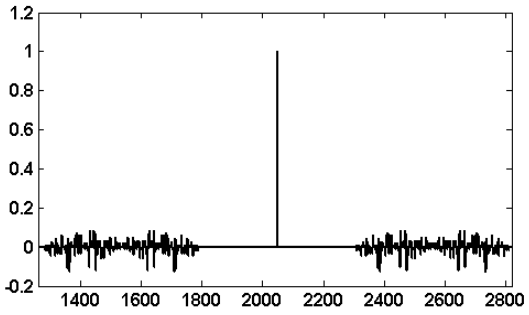

Fig. 4 Simulation result of proposed MF output

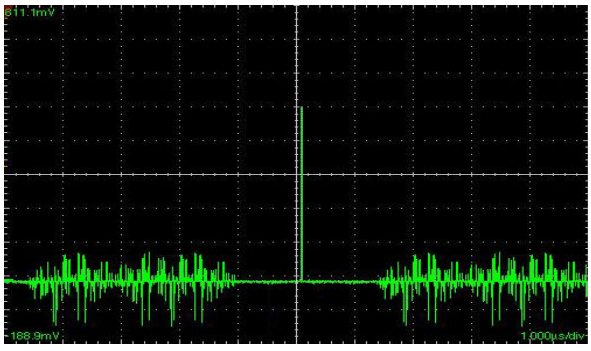

Fig. 5 Measured result of proposed MF output