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Enhancement-Mode High Electron Mobility Transistors Lattice-Matched to InP Substrates Utilizing Ti/Pt/Au Gate Metallization

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Abstract

Enhancement-mode high electron mobility transistors (EHEMTs) were fabricated on $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterostructures grown on InP substrates. Vertical scaling of heterostructures enabled the realization of positive threshold voltage with Ti/Pt/Au gates. The fabricated EHEMTs with 0.18 μm-gates exhibited threshold voltage of 100 mV, peak transconductance of 810 mS/mm, and 150 GHz of unity current gain cut-off frequency (f_T).

Introduction

In the fabrication process of EHEMTs on heterostructures lattice-matched to InP, the most critical fabrication process is the formation of gate electrodes on InAlAs/InGaAs heterostructures to achieve positive threshold voltages. Buried-Pt gate have conventionally been utilized to realize EHEMTs on InP substrates [1-6]. However, there are potential problems in buried-Pt gates [7-8]. The reliability of Pt-based gates on InAlAs is problematic under the elevated temperature due to the continuous shift in threshold voltage induced by the continous sinking properties of Pt-based gate metallization. Pt also has property to diffuse into semiconductor layer in a spike which can result in permanent device failure.

In this study, the gate electrodes have been fabricated with conventional Ti/Pt/Au metallization which have been widely utilized in DHEMTs technologies for comercial products. This gate metallization has been proven to be stable and the penetration depth of Ti into semiconductor was constant under the high temperature life test [9]. Heterostructures for HEMTs were vertically scaled to achieve positive threshold voltages with Ti/Pt/Au gate metallizaiton and their performance were compared with those of EHEMTs with Pt/Ti/Pt/Au metallizations.

Experiments

To achieve positive threshold voltage for EHEMTs, there can be two ways for the heterostructures with the same sheet carrier concentration n_s. One is utilizing high Schottky barrier, ϕ_B, and the other is scaling down the effective thickness of Schottky layer, d_d. Buried-Pt gate have been utilized to achieve high Schottky barrier height as well as to reduce d_d [1,3,5,6].

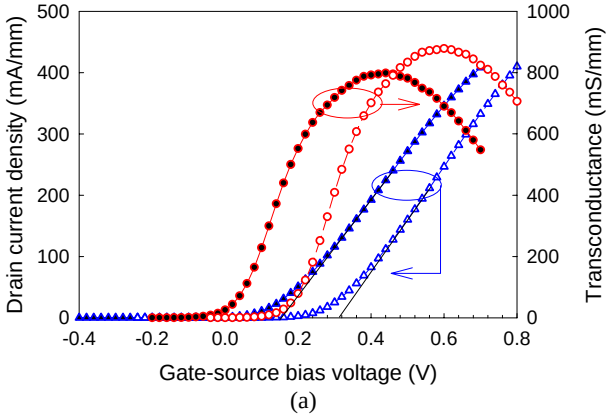
When the gate metallization changes from Pt to Ti, ϕ_B changes because Ti-based Schottky contacts have lower barrier height (~0.7 eV) compared with buried-Pt Schottky contact (~0.85 eV). The difference in barrier height ϕ_B should be compensated by vertically scaling d_d or reducing n_s. If the n_s be reduced, drain current density and transconductance are to be reduced, which it is not desirable for high speed and high power applications.

As is described in reference (3), the thickness of Schottky layer was 120 nm, and the sheet carrier density was $1.0\times10^{12}/cm^2$ for the previous EHEMTs. To improve the current driving capability, the sheet carrier density was increased to be $1.5\times10^{12}/cm^2$. To compensate the lower Schottky barrier height by employing Ti/Pt/Au gate metallization and to deplete the increased channel carriers, the heterostructure for HEMTs layer have been vertically scaled to achieve positive threshold voltages according to equation (1). The Schottky layer thickness was scaled down from 12 nm to 6 nm to achieve positive threshold voltage in this study.

For comparative study, Ti/Pt/Au and Pt/Ti/Pt/Au gates were fabricated on the same HEMT heterostructures. The detailed fabrication process can be found elsewhere [3]. Current-voltage transfer characteristics of HEMTs with Pt/Ti/Pt/Au and Ti/Pt/Au are shown in Figures 1 (a) and (b), respectively.

When the gates are annealed at an elevated temperature of 270 ^oC for 30 sec to stabilize the gate metallization, the threshold voltage was shifted in the positive direction, and the peak transconductance value increased due to the increased Schottky barrier heights as well as the reduced effective thickness of the Schottky layer. Compared with Pt/Ti/Pt/Au gate metallization, Ti/Pt/Au metallization had resulted in the smaller threshold voltage shift and the smaller increase in transconductance, which indicate that the penetration depth of Ti is less than that of Pt and the enhancement of Schottky barrier height is also the smaller for Ti/Pt/Au metallization. The peak transconductances were measured to be 810 mS/mm and 880 mS/mm for Ti/Pt/Au and Pt/Ti/Pt/Au gates, respectively.

By scaling down the vertical heterostructure, positive threshold voltage could be obtained. When the Pt–gate was annealed, threshold voltage was measured to be 0.3 V, which is too high



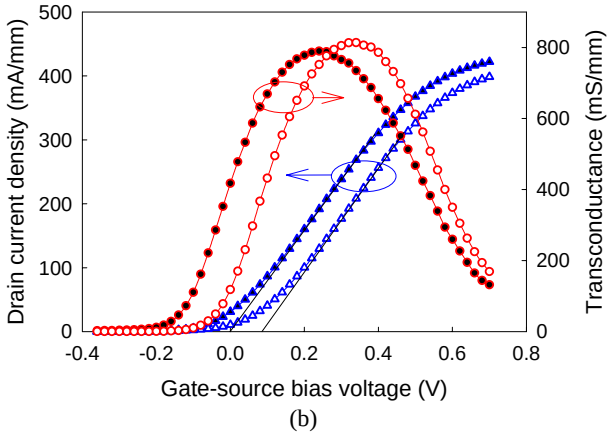


Fig. 1 Voltage-current transfer characteristics of EHEMTs with Pt/Ti/Pt/Au (a) and Ti/Pt/Au gate metallizations (b).

because input voltage swing will be limited, whereas Ti/Pt/Au gates resulted in ~100 mV with I_{dss} of 10 mA/mm.

High drain current of ~ 400 mA/mm was achieved, which is an improvement over the 250 mA/mm obtained from previous devices. The devices also exhibited excellent pinch-off characteristics.

RF characteristics were also measured for these two types of devices. Devices were measured at the gate bias voltages which lead to maximum $g_{m,}$ and the drain bias voltage was set to 1.5 V. The results are shown in Figure 2. The unity-current gain cutoff frequencies (f_T) were measured to be 150 GHz and 100 GHz for devices with 0.18 µm Ti/Pt/Au and Pt/Ti/Pt/Au gates, respectively. Before gate-annealing, Pt-gate device also exhibited similar performance with f_T of 150 GHz. However, f_T decreased a lot and exhibited only 100 GHz when they were annealed. It is due to the increased gate-to-source capacitance through the reduced thickness of effective Schottky layer. The C_{gs}'s extracted from S-parameter measurements were 590 fF/mm and 850 fF/mm for Ti/Pt/Au and Pt/Ti/Pt/Au gate HEMTs, respectively.

Thermal stability of the gate metallization has been studied for both the devices at an elevated temperature. The changes in the threshold voltage as well as the peak transconductace values for Ti/Pt/Au devices are much smaller than those for buried-Pt devices.

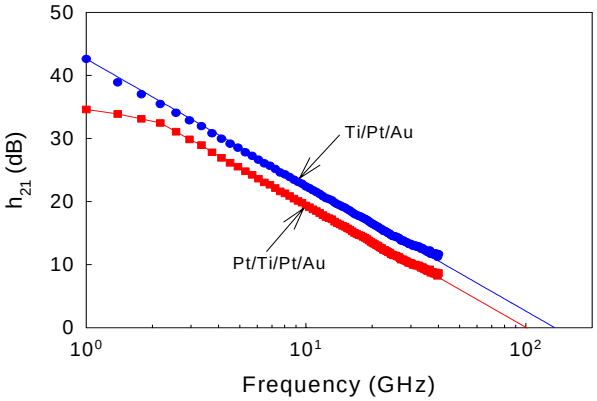


Fig. 2 Microwave characteristics of EHEMTs with Pt/Ti/Pt/Au and Ti/Pt/Au gate metallizations.

Conclusion

Enhancement-mode HEMTs were fabricated using Ti/Pt/Au gate metallization. Positive threshold voltage was achieved through the vertical scaling of EHEMT heterostructures. Their DC and RF performances are as good as EHEMTs with buried-Pt gate with thicker Schottky layer. The thermal stability of Ti/Pt/Au EHEMTs was found out to be better than the buried-Pt gate devices, and the results will be presented.

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