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HEMT Yield Improvement with Ultrasonic-assisted recess for High speed Integrated Circuit

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1. Introduction

InP-based InAlAs/InGaAs high-electron mobility transistors have been a great contribution on the research and development of high speed Integrated Circuits, due to higher electron mobilities, saturation velocities, and sheet electron densities [1]-[2]. In the Integrated Circuit using HEMT as active device, Gate recess process has considerable influence upon yield and uniformity. Uniform initial reaction between InGaAs cap layer and wet etchant plays an important role in yield and uniformity

In this paper we present ultrasonic-assisted recess method to promote uniform initial reaction in recess process. This method enables to achieve high yield and uniformity in the Integrated Circuit. The HEMT fabricated using ultrasonic-assisted recess is compared with conventional process in yield and uniformity

2. Epitaxial structure

This work deals with $In_{0.65}GaAs/In_{0.52}AlAs$ Pseudomorphic HEMT grown by molecular beam epitaxy (MBE) on a InP substrate , yielding a mobility of 10,500 cm^2/V-s and a sheet carrier density of $3.3x10^{12}/cm^2$ at 300K. The epitaxial structure was shown in Fig. 1. To get lower ohmic contact resistance, we adopted the multi-cap layer with high doping concentration($2x10^{19}cm^{-3}$) and 720Å total thickness [3]. Between cap and barrier InP layer was inserted as etch stop layer for high yield and uniformity.

3. Ultrasonic-assisted gate recess

To optimize recess process with ultrasonic, the 0.1-um T-gates were defined by electron beam lithography using ZEP/PMGI/ZEP tri-layer and double exposure/double develop. After the definition of T-gates, Si_3N_4 layer below ZEP/PMGI/ZEP tri-layer was reactive ion etched(RIE) in SF_6/Ar Gas. Selective etchant(solution of citric acid and Hydro-peroxide) was used for recess condition optimization with ultrasonic. Without ultrasonic, the citric acid etches away $In_{0.53}GaAs$ layer with 1400Å/min etch rate and has high selectivity for InGaAs/InP. Fig. 2 shows InGaAs layer etch depth by citric acid with ultrasonic on various condition. Etch rate by the citric acid in InGaAs layer is remarkably increased with ultrasonic because of promoted reaction between etchant and cap layer. For InGaAs layer Etch characteristics by citric acid are shown in Fig. 3. when power and frequency of ultrasonic is decreased, etch direction of InGaAs layer is changed from vertical to horizontal direction. We adopted first condition with 5sec in Fig. 2 because etch in horizontal direction attacks InP etch stop layer less than vertical direction. Additional recess time without ultrasonic was 30sec. Thus final side recess length was 100nm which was optimum condition in previous experiment.

3. Device characteristics

Integrated Circuit using 0.1-μm InGaAs/InAlAs HEMTs was fabricated with ultrasonic-assisted recess condition. HEMTs in the Integrated Circuit were measured on wafer for DC and RF performance. The DC characteristics are shown in Fig. 4. The curve indicated no kink effect and no reduction of saturation current with ultrasonic recess. Device had the DC characteristics of Vth=-0.76, Gm.max = 1.2S/mm. Unit current gain frequency f_T of 250GHz (V_{ds}=0.8V) were extrapolated from the H_{21}.

4. Yield and uniformity

Yield of measured HEMTs in the Integrated Circuit was 80% without ultrasonic. Using optimized recess condition with ultrasonic HEMT yield of 99% was achieved. Fig. 5 shows threshold voltage dispersion of measured HEMTs. Standard deviation of Vth was improved from 56.44mV to 20.18mV with high uniformity

5. Conclusion

In this paper, ultrasonic-assisted recess method was introduced for HEMT yield improvement in the Integrated Circuit. Through optimization of etch condition, HEMT yield was improved by 19% and standard deviation of threshold voltage in HEMTs was decreased to 36% in comparison with non-ultrasonic recess process

Acknowledgements

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References

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cap	$In_{0.65}GaAs$	100Å	$2e19cm^{-3}$
	$In_{0.53}GaAs$	400Å	$2e19cm^{-3}$
	InP	20Å	$5e18cm^{-3}$
	$In_{0.53}GaAs$	200Å	$2e19cm^{-3}$
Etch stop	InP	40Å	undoped
Barrier	$In_{0.52}AlAs$	80Å	undoped
δ-doping	Si		$5e12cm^{-2}$
spacer	$In_{0.52}AlAs$	40Å	undoped
channel	$In_{0.65}GaAs$	100Å	undoped
	$In_{0.53}GaAs$	100Å	undoped
Buffer	$In_{0.52}AlAs$	5000Å	undoped
substrate	S.I. InP Sub.		undoped

Fig. 1. HEMT epitaxial layer structure with multi-cap layer for lower contact resistance

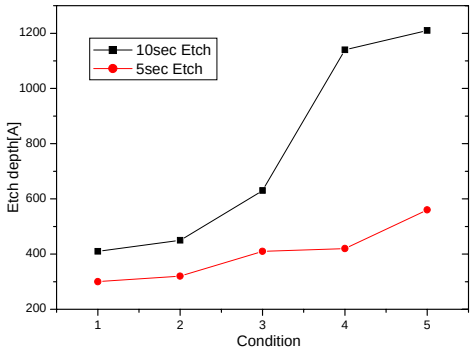
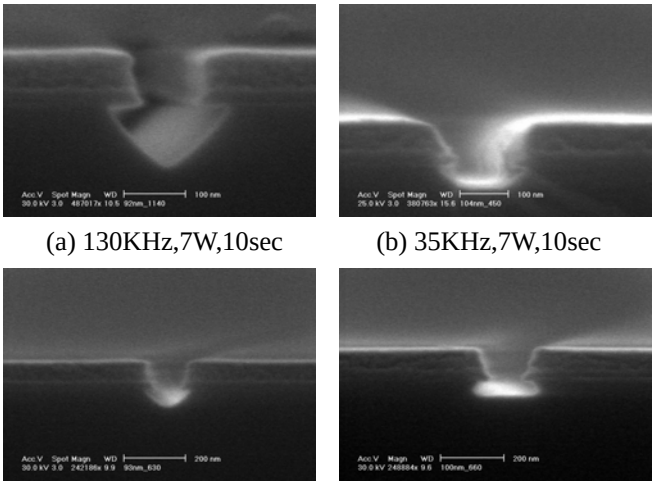


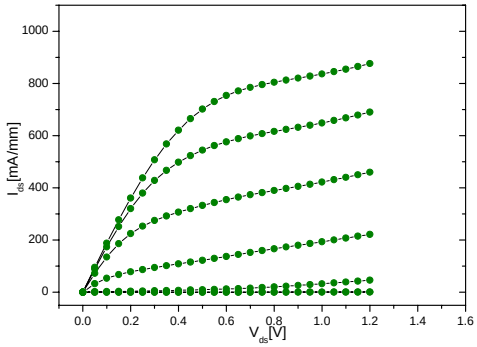
Fig. 2. Etch Depth profile using Ultrasonic-assisted recess with various condition
(condition 1: 35Khz, 3.5W
condition 2: 35KHz, 7W
condition 3: 35KHz, 19W
condition 4: 130KHz, 7W
condition 5: 130KHz, 19W)



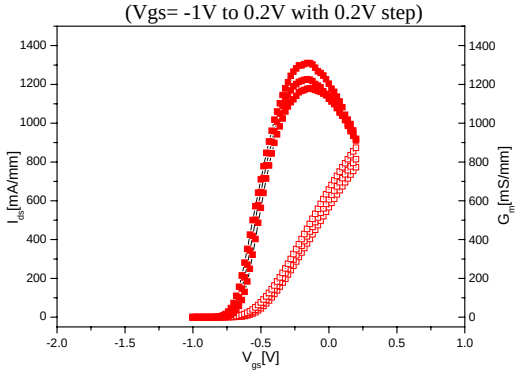
(a) 130KHz,7W,10sec (b) 35KHz,7W,10sec

(c) 35KHz,19W,10sec (d) 35KHz,3.5W,10sec

Fig. 3. Ultrasonic-assisted recess profile of InGaAs layer with various condition (Frequency, power, time)

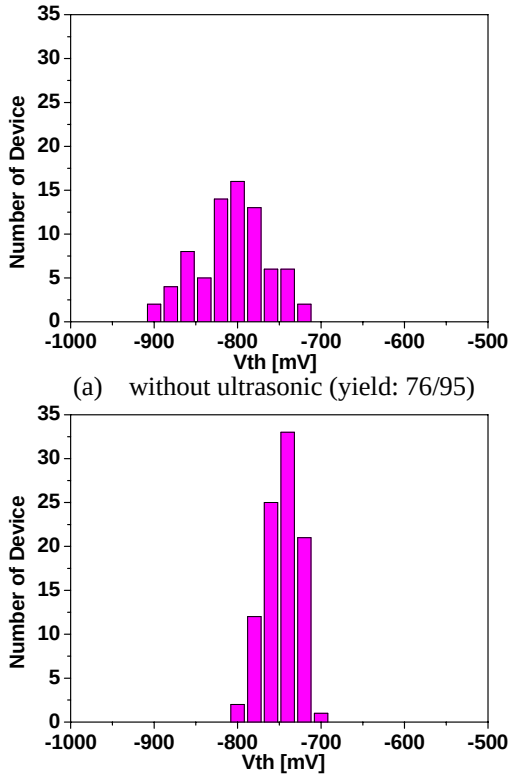


(a) DC I-V characteristics
(Vgs= -1V to 0.2V with 0.2V step)



(b) Transconductance characteristics
(Vds= 0.8V to 1.2V with 0.2V step)

Fig. 4. DC characteristics with ultrasonic-assisted recess



(a) without ultrasonic (yield: 76/95)

(b) with ultrasonic (yield: 94/95)

Fig. 5. Threshold voltage dispersion comparison