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A Comparative Study on the DC, Microwave Characteristics of 0.12 μm Double-Recessed Gate AlGaAs/InGaAs/GaAs PHEMTs Using a Dielectric Assisted Process

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1. Introduction

Pseudomorphic high electron mobility transistors (PHEMTs) are promising devices for millimeter-wave and optical communications systems due to their excellent high frequency and low-noise performance. In order to further improve the performance of the devices, their gate length must be reduced down to the technological limit [1].

In this study, we demonstrate the fabrication of 0.12 μm double-recessed T-gate AlGaAs/InGaAs/GaAs PHEMTs using a PECVD SiN_x-assisted process. It will be shown that 0.12 μm T-gate PHEMTs fabricated using this process exhibit good DC and microwave characteristics. We report the results on using the two different etching techniques to obtain double-recessed T-gates with 0.12 μm gate lengths.

2. Experimental Details

The PHEMT epitaxial structure was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate and consists of the following layers : 5000 Å GaAs buffer, 30 periods of AlGaAs/GaAs supperlattice buffer, an undoped $Al_{0.23}Ga_{0.77}As$ buffer, silicon planar doping (1×10^{12} cm^{-2}), a 20 Å $Al_{0.23}Ga_{0.77}As$ spacer, a 120 Å $In_{0.2}Ga_{0.8}As$ channel, a 35 Å $Al_{0.23}Ga_{0.77}As$ spacer, silicon planar doping (4.5×10^{12} cm^{-2}), a 250 Å $Al_{0.23}Ga_{0.77}As$ Schottky contact layer. Finally, a 400 Å n-type doped GaAs cap (5×10^{18} cm^{-3}) layer was grown to protect the active layer from the oxidation, causing the creation of defects [2]. The mesa was defined by conventional photolithography. The ohmic contact alloying was performed by two-step annealing, first at 340℃ and then at 380℃, for 20 s each. The steps of the fabrication of double-recessed T-gate using a SiN_x -assisted process are outlined schematically in Fig. 1. A 300 Å SiN_x layer was deposited by PECVD at 260℃ to protect the device and to support the gate. Then, a wide recess is formed by dry or wet etching using a photoresist as a mask. In this step, the SiN_x layer was etched by RIE (sample A) or BOE (sample B), and the GaAs cap layer was etched by ECR (sample A) or H_3PO_4-based wet etching (sample B). Next, a 200 Å SiN_x layer was deposited, and the SiN_x layer was etched by RIE to create a 0.12 μm gate footprint. The gate footprint patterning was done by electron beam lithography using a Leica EBPG 5000 plus system. The top of the T-gate structure which consists of a

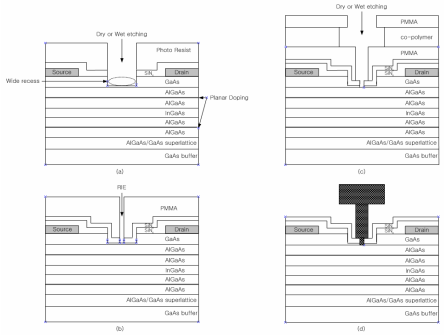


Fig. 1. Cross-sectional schematic view of 0.12 μm double-recessed T-gate PHEMTs fabrication process.

wide head part and a narrow lower layer(0.3 μm) has been employed taking advantages of its large cross-section area of the gate and mechanically stable structure. The gate recessing of the device was performed using a ECR (sample A) or H_3PO_4-based wet etching (sample B) process. After the gate recess, Ti/Pt/Au layers were deposited and lifted-off. Figure 2 shows a SEM image of the cross-section of a fabricated double-recessed T-gate PHEMT taken from an actual device.

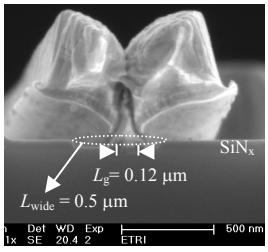


Fig. 2. SEM photograph of the cross section of a double-recessed T-gate PHEMT.

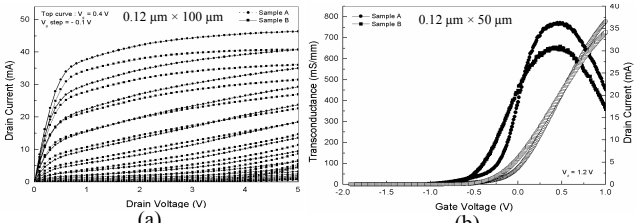
3. Results and Discussion

PHEMTs with source-to-drain spacings of 2.5 μm, source-to-gate spacings of 0.79 μm, gate-to-drain spacings of 1.59 μm, unit gate widths of 50 μm and two gate fingers, gate lengths of 0.12 μm were fabricated using the tri-layer resist on the PHEMT structure described earlier. This asymmetric source and drain structure with shorter gate-to-source separation than gate-to-drain can be applied for reducing the source resistance. The DC and RF characteristics were evaluated by measuring the devices in a HP 4156B DC parameter analyzer and a HP 8510C network

analyzer, respectively.

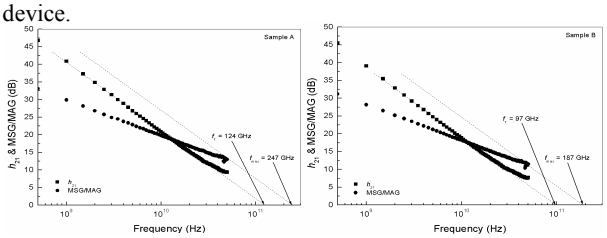
Figure 3(a) shows drain current as a function of source-to-drain voltage (V_{ds}) for 0.12 μm PHEMTs fabricated by dry and wet etching. The devices exhibited good pinch-off characteristics. We obtained a pinch-off voltage of V_p = - 0.86 V, and a drain-source saturation current (I_{dss}) of 24 mA at V_{gs} = 0 V and V_{ds} = 5 V for sample A. In case of sample B, the pinch-off voltage of V_p = - 0.68 V, and a drain-source saturation current (I_{dss}) of 23 mA at V_{gs} = 0 V and V_{ds} = 5 V. The extrinsic transconductance (g_m) and drain current (I_{ds}) as a function of source-to-gate voltage (V_{gs}) at 1.2 V of drain voltage were measured and shown in Fig. 3(b). The maximum g_m was measured as 765 mS/mm for sample A and 650 mS/mm for sample B at V_{gs} = 0.4 V.

The RF properties of the fabricated PHEMTs were measured by on-wafer probing from 0.5 to 50 GHz. Typical current gain (h_{21}), maximum stable and available gain (MSG/MAG) as a function of frequency for sample A are shown in Fig. 4(a). The drain and gate voltages applied in the RF measurements were 1.2 and 0.4 V, respectively. From the measured S-parameters, the small-signal equivalent circuit was extracted using a direct extraction technique and the corresponding f_T and f_{max} were estimated. Both f_T and f_{max} were calculated using the h_{21} and MSG/MAG values by an extrapolation of – 20 dB/decade slope. The current gain cut-off frequency (f_T) was 124 GHz and the maximum oscillation frequency (f_{max}) was 247 GHz. Current gain h_{21} and MSG/MAG as a function of frequency for sample B are shown in Fig. 7(b). The extrapolated cut-off frequency f_T and the maximum oscillation frequency f_{max} were 97 GHz and 187 GHz, respectively.



(a) (b)

Fig. 3. (a) Drain current as a function of source-to-drain voltage and (b) the extrinsic transconductance and drain current as a function of source-to-gate voltage for the fabricated 0.12 μm PHEMT device.



(a) (b)

Fig. 4. Measured current gain and maximum available gain as a function of frequency for the fabricated 0.12 μm PHEMT devices. (a) dry etching; (b) wet etching.

This result was comparable or better values than the previously reported values for a conventional PHEMT process [3]-[5]. In order to investigate the increase of cut-off frequency for sample A, the parameters in the small signal equivalent circuit model were extracted at the maximum transconductance bias point and shown in Table 1. The fitting frequency range for extrapolation was 10 ~ 40 GHz. In case of sample A, the improvement in RF performance can be understood in terms of the decrease in parasitic capacitances and increase of the transconductance due to dielectric and gate recess etching method. This method is promising in solving the problem of decreasing the parasitic capacitance for short gate lengths as well as obtaining a mechanically stable double-recessed T-gate structure. However, it must be mentioned that the etching of the SiN*x* is critical. The SiN*x* is etched off before the gate recess is done because a certain amount of overetch in RIE is required. The degree of overetch must be controlled to prevent ion-induced damage in the gate area.

Table 1. Small signal equivalent circuit parameters at V_{ds} = 1.2 V and V_{gs} = 0.4 V. The parameters were obtained by equivalent circuit analysis.

Device	L_g (μm)	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_g (Ω)	R_s (Ω)	R_i (Ω)	R_d (Ω)	τ (ps)
Sample A	0.12	89	101	13.3	37.6	1.0	1.4	5.7	0.7	0.6
Sample B	0.12	78	120	19.2	36.1	1.3	2.5	5.9	0.5	0.8

4. Conclusions

The fabrication of a 0.12 μm double-recessed T-gate PHEMTs with the SiN*x* assisted process has been described. The gate footprint pattern is transferred into the SiN*x* layer by RIE in CF_4 plasma. The gate recessing was carried out two different etching techniques to obtain double-recessed T-gates with 0.12 μm gate lengths. The cut-off frequency and the maximum oscillation frequency of a double recessed PHEMT device using a dry etching process were 124 and 247 GHz, respectively. We believe that the double-recessed technology using a dry etching process will lead to possible millimeter-wave applications and good characteristics. We are now developing the GaAs PHEMT MMIC based on the results using a dry etching process for microwave and wireless applications on 4-inch wafer.

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