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Compact RF Switches Using Dielectric Overhang Gate Process & Stacked Inductor

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In this paper we present two fabrication techniques for compact RF switches with small area. The first is dielectric overhang gate process which enables us to reduce the distance between source electrode and drain electrode of multiple gate HEMT. The fabricated quadrate gate Single Pole Double Throw (SPDT) switch MMIC had the insertion loss of 0.4dB and the isolation of 20dB at 900MHz while it consumed the area of 0.15mm^2. The second is the inductor stacking technology for LC resonance. Multilayer Inductor is stacked on top of the switch transistor. It improves the isolation without consuming extra area.

KEYWORDS: switch, multiple, gate, HEMT, dielectric, overhang, LC, resonance, BCB,

1. Introduction

Switch is an important microwave component for time-division multiple access (TDMA) system such as GSM and DCS. There is a growing need for low cost, low loss RF switch according to the trend of multi-band and multi-functionality of mobile communication devices.[1] The cost is a primarily important consideration point in selecting switch. The chip size determines the cost of switch IC.

Layout parameters such as the length of ohmic contact are important factors for smaller chip size. Reducing the length of ohmic contact is a way to improve the isolation. [2] Reducing the distance between source electrode and drain electrode results in the increase of source to drain capacitance. [2] We found out that reducing the length of ohmic electrode and the distance between source electrode and drain electrode is better for overall switch performance and small area consumption. To cope with the high power of GSM, multiple gate FET technology is often used. [3] But it is not easy to reduce the distance between source electrode and drain electrode of multiple gate HEMT. If the two electrodes are too close, the multiple gate resists profile is easy to collapse. We developed dielectric overhang gate process for multiple gate HEMT, which enables us to reduce the distance between source electrode and drain electrode. The fabricated 0.15um quadrate gate Single Pole Double Throw (SPDT) HEMT switch had the loss of 0.4dB and the isolation of 20dB while consumed the area of only 0.15mm^2.

LC resonance was used in order to enhance isolation of switch. [4] However inductors usually take up large area. A way to save area is to stack inductor over the transistor. We developed inductor stacking technology for LC resonance. As a multilayer inductor is stacked on top of the switch transistor, no extra area but for the area for VIA contact is need.

2. Dielectric overhang gate process

In order to reduce the distance between source and drain of multiple gate HEMT, it is important to reduce the gate to gate distance. Resist profile for multiple gate is easy to collapse if the gate to gate distance is reduced down to 1μm. Dielectric is mechanically more stable than photo-resists. Dielectric layers of Si_3N_4/SiO_2 were used for overhang profile. The fabrication sequence is as follows. At first Si_3N_4 of 1000Å and SiO_2 of 300Å were deposited in sequence. 1000Å thick ZEP was coated on it. 0.1μm gate was patterned on ZEP using e-beam lithography. CF_4/H_2 mixture was used to etch away dielectric materials in vertical direction. After the first etch using CF_4/H_2 gas, Si_3N_4 of 400Å remained. And then SF_6/Ar was used to isotropically etch away Si_3N_4. The etch selectivity of Si_3N_4 to SiO_2 using SF_6/Ar plasma is 20:1. SiO_2 is seldom etched by SF_6/Ar plasma. Figure 1 (a) and (b) show the schematic diagram and the scanning electron microscope (SEM) image of the dielectric overhang profile. Using dielectric overhang process the gate to gate distance could be reduced down to 0.25um. The fabricated quadrate gate SPDT switch MMIC of figure 1 (c) had the insertion loss of 0.4dB and the isolation of 20dB at 900MHz while it consumed the area of 0.15mm^2.

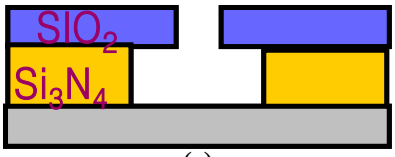
3. LC resonance with stacked inductor

LC resonance switch has the merit of improved isolation and the demerit of large area consumption. We developed inductor stacking technology for LC resonance with double layer

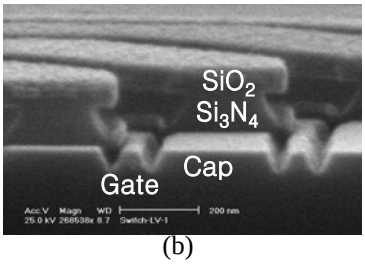
inductor stacked on top of the switch transistor. Benzocyclobutene (BCB) was used for multilayer process for its low dielectric constant. Figure 2(a) and (b) show the schematic diagram and the scanning electron microscope (SEM) image of the transistor with stacked inductor. EM simulation showed us that the major coupling effect of stacking is the reduction of inductance and deterioration of Q factor of the inductor. In order to reduce the coupling effects, inductor should be place as high as possible. We placed the inductor 7μm above the transistor. We fabricated a 2mm transistor with stacked inductor. It is not a complete switch yet. Figure 2 (c) shows the isolation of 2mm transistor with stacked inductor as a function of frequency. At 2.7GHz resonance occurred and isolation improved by 7dB at that frequency.

4. Conclusion

We developed two fabrication techniques for compact RF switch. With dielectric overhang gate process, the source to drain distance of multiple gate HEMT could be reduced. Stacked inductor process could improve isolation at resonance frequency without much increase of area.



(a)



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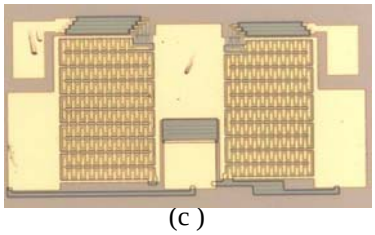
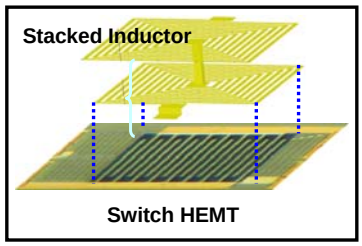
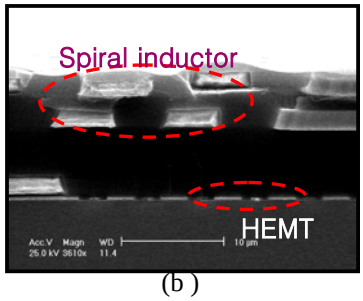


(c)

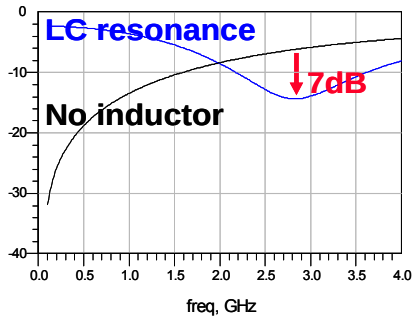
Fig. 1 (a) Schematic diagram of SiO_2/Si_3N_4 dielectric overhang (b) SEM image of quadrate gate (c) top view of the fabricated SPDT switch



(a)



(b)



(c)

Fig. 2 (a) Schematic diagram of stacking inductor (b) SEM image of the transistor with stacked inductor (c) isolation as a function of frequency

Acknowledgements

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