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Nanowire Field Effect Transistor

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1. Introduction

Semiconductor nanowires may have the potential to extend the semiconductor technology road map. The radial strain relaxation in the wires allows a heterogeneous materials integration and novel heterostructures to be incorporated which may be used to improve the contact resistance and to design the channel material for optimal transport properties. The wire geometry further allows wrap-gates to be formed, by which the channel potential efficiently may be controlled. However, a remaining key issue for the nanowire technology is to demonstrate a parallel processing scheme that allows device quality fabrication. Also, the design of the heterostructures in the channel must be considered.

We report on the development of a vertical nanowire InAs MISFET [1-4]. The nanowires have been grown by Chemical Beam Epitaxy (CBE) and the transistors have been processed by a number of subsequent etching and deposition steps. The 0.8 µm gate-length transistors show a good current saturation and a low saturation voltage. We also describe the benefits of introducing a heterobarrier into the nanowire to increase the current on/off ratio.

2. Processing

Matrixes (11*x*11) of gold particles were formed by electron beam pattering and deposition on a {111} InAs substrate. Following lift-off, the nanowires were grown by CBE at a temperature of 490 °C to a total length of 3 µm. Deposition of SiN_x by ICP-RIE (40 nm) followed by sputtering of a Ti/Au gate was as the isolating layer and the gate metal, respectively. The sample was then spin-coated with a resist followed by an etch-back to a thickness of 0.8 µm and a wet etch of the gate metal to define the gate length. Finally, an airbridge technology was employed to contact the top of the wires (drain contact), while the substrate acted as a source contact. In total, this transistor processing scheme consisted of one electron-beam lithography step (definition of wire position prior to the growth) and solely three optical lithography steps, which were used in combination with the standard deposition and etching steps to process the complete transistor.

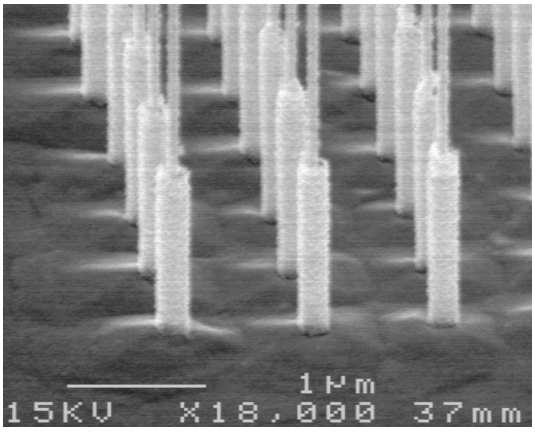
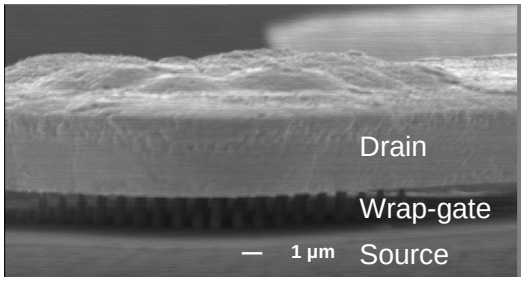


Fig. 1 Array of nanowires after gate formation.



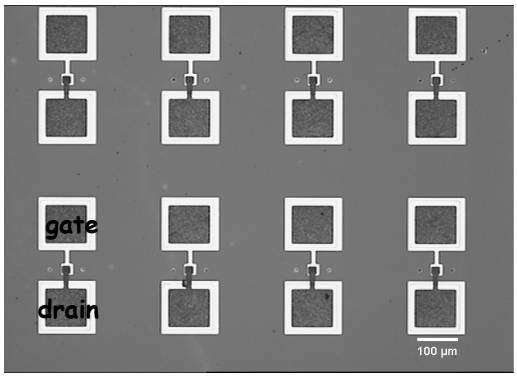


Fig 2 Airbridge (top) and device layout (below) of the completed transistor.

3. Characterization

The transistors were characterized at room temperature in a common source configuration. The transistor in Fig. 3 shows a drive current of 1 mA at V_g=2.2 V and a current saturation at V_{sd}=0.4 V. Other transistors with only 40 nanowires but the same gate-length, showed a drive current of 100 µA at V_g=0 V with a threshold voltage of V_{th}=-0.15 V. These transistors also showed a subthreshold slope of 100 mV/decade and a maximum

current on/off ratio of 10^3. All transistors exhibit charging effects related to the SiN_x layer, which makes the evaluation of the transport properties, like the mobility, difficult. Even so, the deduced value for the mobility in the range of 10000 cm^2/Vs may be realistic.

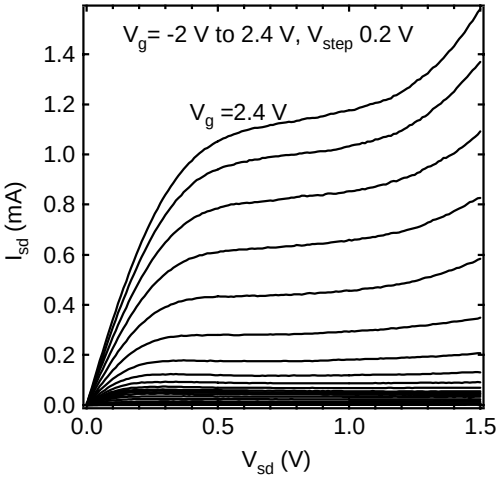


Fig 3 Room temperature characteristics of nanowire transistor consisting of 100 nanowires in parallel.

4. Heterostructure nanowire transistors

In order to evaluate the potential performance of scaled nanowire transistors, simulations of 100-nm-gate length wrap-gated transistors have been performed within the drift-and-diffusion formalism [5]. In the InAs transistor, a heterobarrier of InAsP has been introduced to block the off current in the center of the nanowire which enhances the current on/off ratio [6]. The input data to the simulations (mobility of 10 000 cm^2/Vs, $v_{sat}=3x10^7$ cm/s) have been obtained from fitting to experimental transistor data. The simulated data suggests that for a gate swing of 0.5 V, the 100-nm-gate-length heterostructure nanowire FETs may achieve a gate delay below 2 ps, an energy-delay product of $5x10^{-28}$ Js/µm, and a subthreshold slope of 60 mV/decade, while maintaining a current on/off ratio above 10^3. These values compare favorably to standard NMOS transistors. To achieve these values a heterobarrier must be introduced to reduce the off current, mainly originating from transport in the center of the wire. According to the simulations, the drive current remains almost constant for a fixed gate overdrive and modest barrier heights. The introduction of the barrier does not increase the gate delay severely. This demonstrates that heterostructure design in the nanowires may be employed to improve the device characteristics and that barriers may be used to tailor the band structure along the current path.

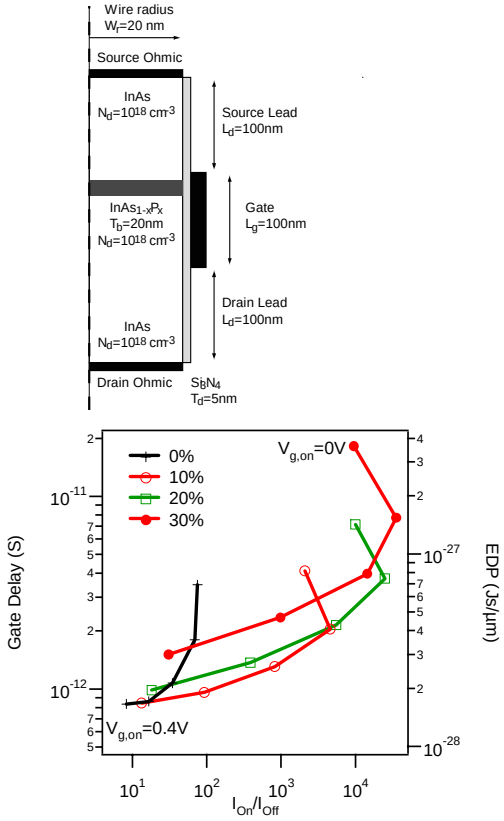


Fig 4 Simulated heterostructure nanowire FET. Design (above) and extracted data for different alloy compositions (P content) and gate voltages (below).

5. Conclusions

A parallel processing technology for vertical nanowire transistors has been developed. The nanowires have been grown in pre-defined positions and optical lithogrhaphy combined with controlled deposition and etching has been used to complete the transistors. The 0.8 µm devices show a good saturation characteristics and drive currents above 1 mA have been achieved for 100 nanowires in parallel. Simulation of scaled devices shows that the introduction of a heterobarrier is essential to suppress the off-current in order to achieve a useful current on/off ratio as the gate swing is reduced to 0.5 V.

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6. References

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