Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 228-229

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CMOS-Compatible Suspended Square Inductors on Silicon Wafers for RF ICs

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1. Introduction

Inductor is a key element in radio frequency (RF) devices. The applications of inductor include filter [1], VCO (voltage-controlled oscillator) [2], and power amplifier [3]. In order to obtain high devices performance, they require inductor with high quality factor (Q-factor). Hence, many researches attempt to increase Q-factor by using low resistivity conductor such as copper to reduce ohmic loss or by utilizing special techniques such as pattern ground shield [4], surface micromachining [5], and bulk micromachining [6] to reduce substrate loss. Among these methods, Q-factor of inductor with pattern ground shield is hardly over 10. Although, bulk micromachining technique can effectively improve Q-factor, it is more complex than surface micromachining technique due to more process sequences. As we know, inductor with less process sequences not only reduces cost but also reduces damage of inductor. In surface micromachining techniques, researchers want to reduce dielectric constant of insulator in order to reduce substrate loss. The best way is to suspended inductor by using air as insulator.

In this paper, we use CMOS-compatible surface micromachining technique and copper conductor to achieve suspended inductor. The high frequency characteristics, Q-factor and inductor were extracted at GHz range. The effects of geometry of inductor, conductor length, inner diameter (din), and pitch on high frequency characteristics are discussed.

2. Experiment

The suspended inductors were fabricated on silicon wafer with resistivity of 10 Ω·cm. In order to isolate the silicon wafer from inductor, the wafer was spin-coated a layer of 15μm-thickness polyimide which was cured at 350°C for one hour. The underpass of inductor was fabricated by sputtering 1000Å-thickness of copper on the polyimide as electroplating seed layer and then using photoresist as underpass mold to electroplate 10μm-thickness copper. The contact via was also fabricated by using photoresist as the mold to electroplate 35μm-thickness copper. The fabrication process of spiral coil is the same as underpass. Finally, the suspended inductor was realized by removing photoresist and etching copper seed layer. The scanning electron microscope (SEM) image of suspended inductor is shown in Fig. 1. The pad structure without inductor (dummy structure) was also fabricated to de-embedding parasitic effect of pad. The S-parameters of the inductors and dummy structures were measured by Hp8510c vector network analyzer system. The measured frequency range is from 0.2GHz to 40GHz. The de-embedding S-parameters are converted to Y-parameters. The Q-factor and inductance are obtained by Equations 1 and 2.

$$L = \mathrm{Im}(1/Y_{11})/2\pi f \quad (1)$$

$$Q = -\mathrm{Im}(Y_{11})/\mathrm{Re}(Y_{11}) \quad (2)$$

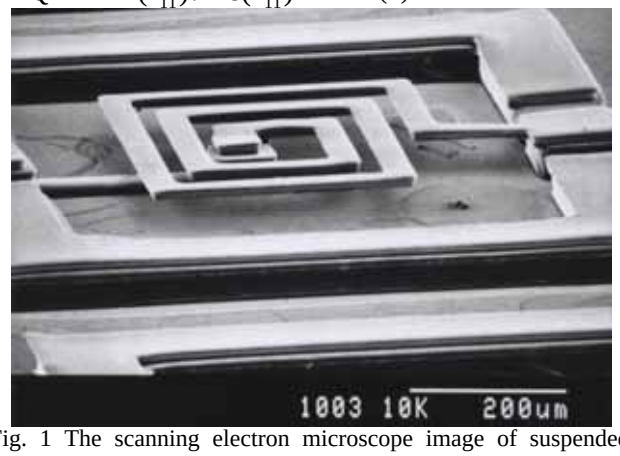

Fig. 1 The scanning electron microscope image of suspended inductor

3. Result and Discussion

The inductors with different pitches and dins were designed and measured on standard silicon substrate. Fig. 2 shows the variation of the inductance as a function of conductor length. The inductor increases in inductance with increasing din or decreasing pitch or increasing conductor length. The rate of the ratio of inductance to conductor length increases with increasing conductor length. These phenomena can be explained by Greenhouse's algorithms. In the Greenhouse's algorithms [7], the inductance includes self-inductance and mutual-inductance. The mutual-inductance can be divided into positive mutual-inductance and negative mutual-inductance. The most important factor of mutual-inductance is the pitch. As conductor length increases, the inductance increases because the self-inductance of a conductor coil is directly proportional to the coil length. The inductor increases in the growth rate of inductance with increasing conductor length because the difference between positive and negative mutual-inductance increases with increasing conductor length. Inductor increases in din and leads to degrade negative mutual-inductance. Inductor decreases in pitch and causes increase in positive mutual-inductance. Hence, inductor with large din and small pitch shows high inductance at the same conductor length.

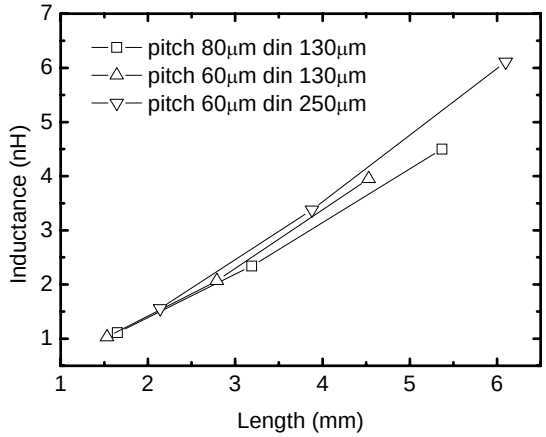

Fig. 2 The measured inductance of inductor with various lengths, pitches and inner diameter.

Fig. 3 shows the measured Q_{max} of the inductors with various lengths, pitches and dins. The Q factor can be represented by lumped-element equivalent circuit.

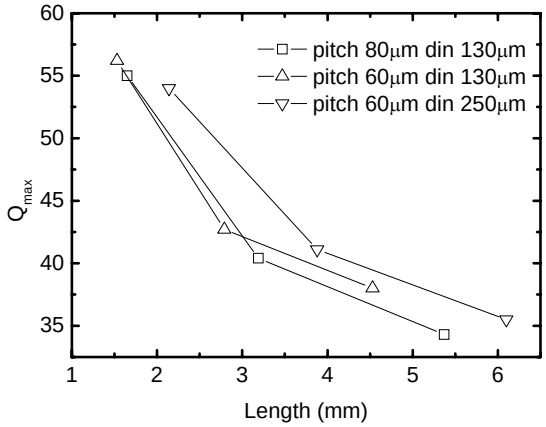

Fig. 3 The measured Q_{max} of inductors with various conductor lengths, pitches and dins.

Fig. 4 shows the lumped-element equivalent circuit of the inductor on Si substrate [8]. In the lumped-element model, L_s and R_s represent the series inductance and the series resistance of the Cu coils, while C_s and C_d the inter-coil capacitance and the parasitic capacitance between the inductor and the Si substrate, respectively. The parasitic resistance and capacitance of the Si substrate are simply modeled by R_{Si} and C_{Si}. For simplification, the three parasitic components, C_d, R_{Si} and C_{Si}, can be reduced into two parameters, C_p and R_p, which are given by

$$R_p = \frac{1}{\omega^2 C_d^{\,2} R_{si}} + \frac{R_{si}(C_d + C_{si})^2}{C_d^{\,2}} \qquad (3)$$

$$C_p = C_d \times \frac{1+\omega^2(C_d + C_{si})C_{si}R_{si}^{\,2}}{1+\omega^2(C_d + C_{si})^2 R_{si}^{\,2}}$$

According to the reduced lump-element model one can deduce the quality factor of the inductor as follows.

$$Q = \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + [(\omega L_s / R_s)^2 + 1] \cdot R_s} \times \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p) \right] \qquad (4)$$

The series resistance and inductance increase at the same time as the length of inductor increases. Compare with inductance, the series resistance has much effect on the first term of Q-factor. Thus, inductor rises in the first term of Q factor with decreasing conductor length. Inductor with long conductor length has large parasitic capacitance and low parasitic resistance in the silicon substrate. Large parasitic capacitance causes decrease in the third term of Q-factor. Low parasitic resistance cause decrease in second term of Q-factor. For this reason, inductor with long conductor length has low Q_{max}. In our experiments, the Q_{max} can be improved by increasing din at the same conductor length. Large din causes increase in inductance and parasitic resistance and decrease in series resistance. These changes improve the first and second terms of Q-factor.

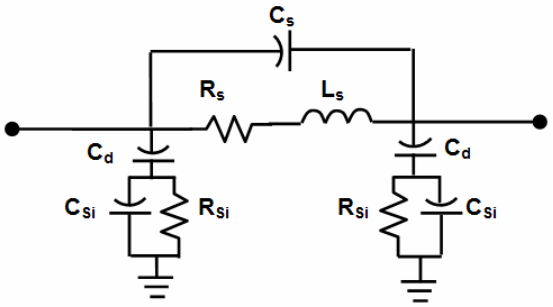

Fig. 4 lumped-element equivalent circuit for inductor.

4. Conclusions

CMOS-compatible high Q factor suspended inductor are successfully designed and fabricated on standard silicon substrate. The effects of geometry of inductors on inductance can be interpreted by Greenhouse's algorithms. The decrease in Q_{max} with increasing conductor length is due to increase parasitic effect and series resistance. It is suggested the inductors with large din and small pitch give raise to better performance.

Acknowledgements

The work is supported by Ministry of Economic Affairs, Technology Development Program for Academia through Grant No. 91-EC-17-A-08-S1-003.

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