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MEMS Wafer Level Packaging by Using Surface Activated Bonding

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1. Introduction

MEMS technology has been attracted much attention because of its microscale. MEMS devices such as a pressure sensor, an accelerometer and a gyroscope, have been commercialized in many kinds of applications such as FA, IT, automobile and medical systems. In considering further downsizing and cost reduction for more portable systems, it is necessary for MEMS devices to provide higher performances with many functions integrated in a small size. Also it is important to reduce the stress in MEMS devices because of an inherently weakness.

MEMS wafer level packaging (WLP) is increasingly important because of suppression for mechanical damages before the dicing, stacked structure, and mass production with lower cost. Anodic bonding technology in a conventional MEMS fabrication has been used in wide applications. However it has serious problems such as the inaccurate alignment, higher stress at the bonding interface, and low productivity, which are caused by the thermal expansion resulted from a bonding temperature of 300-400℃. Surface activated bonding method (SAB) based on the adhesive force across two clean solid surfaces has been proposed as a room temperature bonding [1-3].

We employed SAB using an argon ion beam, and demonstrated low stress and high airtightness diaphragm by WLP.

2. Experiment

In this experiment, a vacuum chamber at the pressure with under 1.0×10^{-5}Pa was used in order bonding two wafers with the following steps i) a surface activation by an argon ion beam, ii) alignment between the wafers by a microscope, iii) wafers pressing. Fabrication procedure of the diaphragms is shown in Figures 1. Diaphragm patterns were delineated by lithographic processes and D-RIE. After bonding the patterned wafer to a cap wafer, an interface between these wafers was observed by a acoustic microscope that detect a void by a reflected ultrasonic wave.

After dicing the wafer pair, airtightness and stress evaluation of the interface were performed. The airtightness was measured by using helium leak detector. The stress was estimated by the peak shift measured with a Raman spectroscope.

3. Results and Consideration

Figures 2 show the acoustic microscope images of the wafers pair with test patterns giving good adhesion. It was found that there was no white area showing a void except the patterned cavities. Figures 3 show photographs of the wafers pair and diaphragms with no damage. It was found that the inside was a vacuum by a concave shape. Diced Chips were obtained in the high yield without damage in the interface and the diaphragms. It was indicated bonding strength sufficient for WLP and the capability of manufacturing varied MEMS devices with a weak structure by these technologies.

The leak rates showing the airtightness of the chips were below 1×10^{-11} Pa m^3/sec the limit of the detection. Figures 4 show the stress as a function of a distance from the interface. The stress near the interface showed the drastically low compared to the anodic bonding and eutectic bonding with an Au-Sn film. It was presumed that the stress caused by the thermal expansion difference between Si and glass after anodic bonding and between Au-Sn alloy and Si after eutectic bonding.

As mentioned above, the low stress and high airtightness on Si/Si bonding were realized and the similar results were obtained on Au/Au bonding. Furthermore, these performances were maintained after high temperature aging and heat cycling.

4. Conclusion

We have demonstrated the diaphragms with low stress and high airtightness by WLP using SAB. We found that the stress near the interface was drastically reduced by using SAB. We showed that the stress near the bonding interface was affected by bonding temperature and that these technologies were very suitable for MEMS required low stress and airtightness, such as bio-sensors and mechanical sensors.

Acknowledgements

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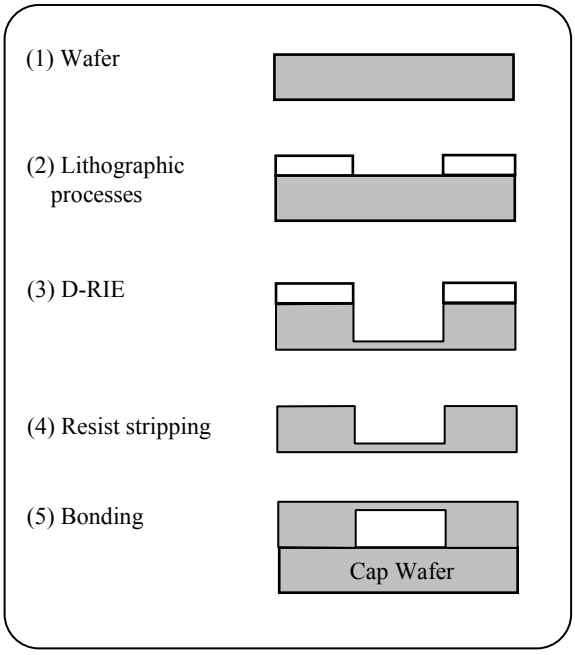

Fig. 1 Fabrication procedure of diaphragms.

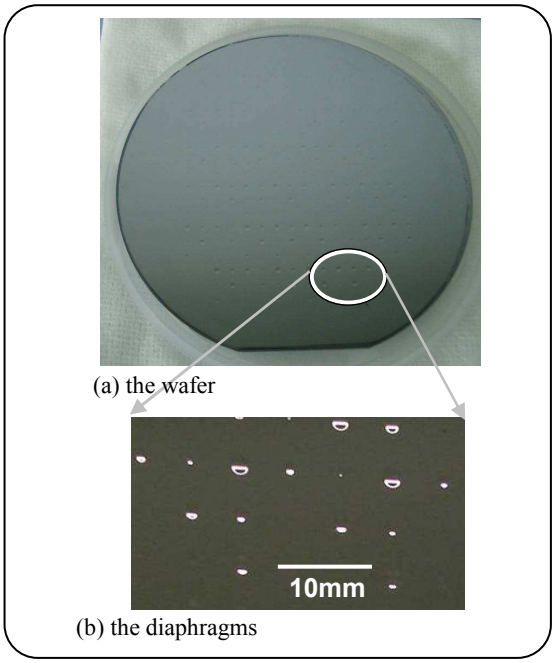

Fig. 3 Photographs of (a) the wafers pairs and (b) the diaphragms.

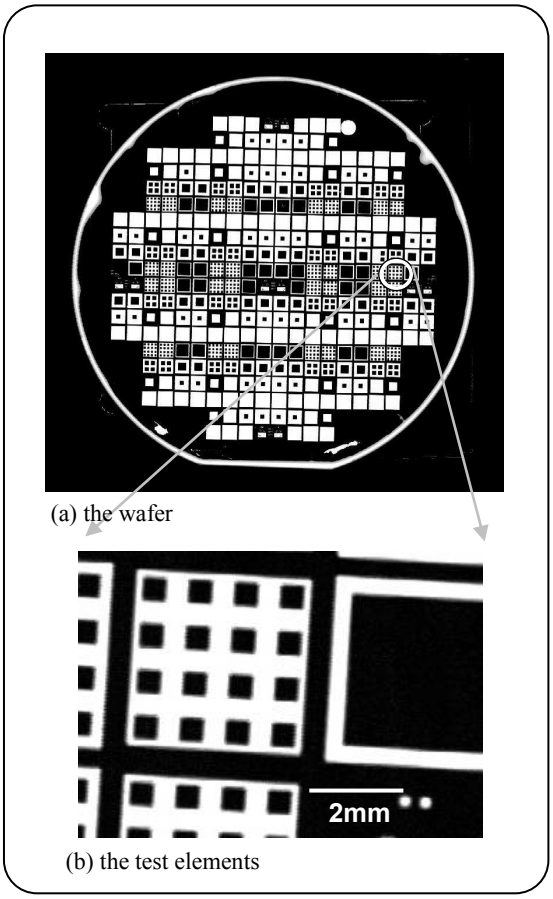

Fig. 2 Acoustic microscope images of (a) the wafers pair and (b) the test elements.

Table. 1 The leak rate of the chip

	Si/Si	Au/Au
Leak rate	1.2×10^{-12}	5.7×10^{-12}

(Pa・m3/sec)

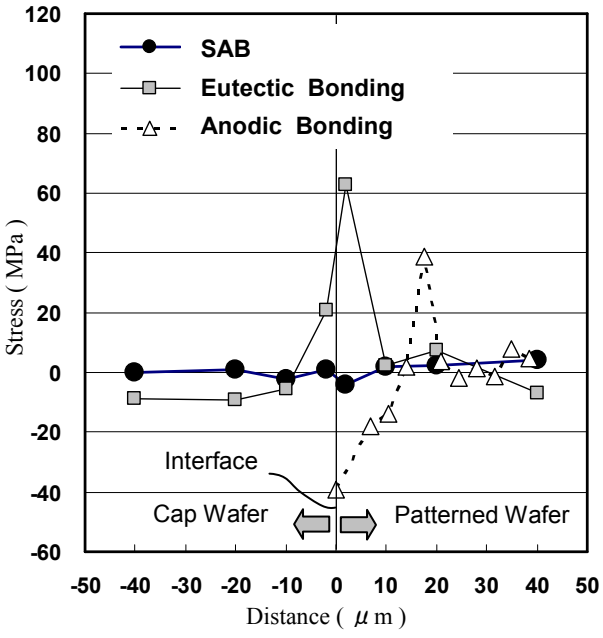

Fig. 4 The stress as a function of the distance from the interface.