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Surface Potential Measurement of Carbon Nanotube FETs using Kelvin Probe Force Microscopy

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1. Introduction

Carbon nanotube field-effect transistors (CNT-FETs) receive considerable attention because of their high-speed potential with a large transconductance. [1]-[2] However, there are many issues which should be addressed such as a hysteresis[3] of the I_D-V_{GS} characteristics and a large parasitic resistance[4]. The surface potential measurement is very effective in studying such phenomena of the CNT-FETs.

In this study, the surface potential of the CNT-FETs was measured using Kelvin probe force microscopy (KFM) [5][6]. A clear potential image of the CNT channel with a diameter of about 1 nm was obtained by the measurement in air. The measured potential image was dependent on the sequence of the gate bias, and showed transient behavior with a time constant of several-tens minutes. It has been demonstrated that these behaviors were consistent with the drain current transient and/or the hysteresis of the current-voltage characteristic of the CNT-FETs.

2. Experiment

Figure 1(a) shows the schematic of the device structure. CNTs were synthesized by microwave plasma-enhanced CVD using position-controlled nanotube growth[7] in which the metal catalyst for the CNT growth was patterned on the substrate using conventional photolithography and metal lift-off processes. An SEM image of the fabricated CNT-FETs with Au electrodes is shown in Fig. 1(b) where the CNT bridges between the source and the drain electrodes. Measured I-V characteristics of the fabricated CNT-FET showed good pinch-off characteristics with a p-type condition behavior.

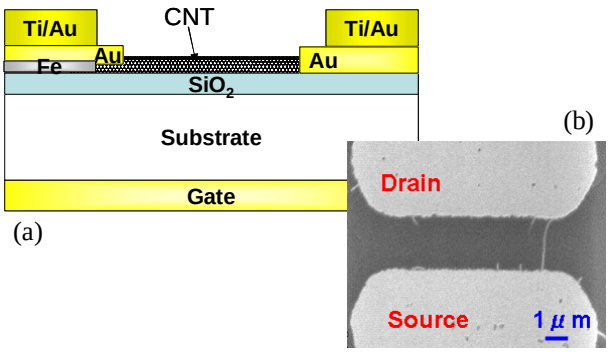

Fig. 1. Schematic device structure (a) and SEM image (b) of the fabricated CNT-FETs.

Figure 2(a) and 2(b) show topographic and surface potential images of the CNT-FET with Au electrodes. A clear potential image is obtained even for the CNT channel with a small diameter of about 1 nm.

Figure 3 shows the surface potential images of the device measured for the various gate bias conditions; (a) V_{GS} = -5 V, (b) V_{GS} = 0 V just after -5 V gate bias stress, (c) V_{GS} = +5 V, (d) V_{GS} = 0 V just after + 5V gate bias stress. (V_{DS} = -0.3 V).

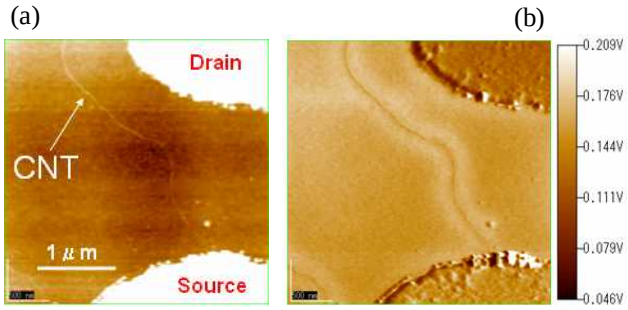

Fig. 2. Topographic (a) and surface potential images (b) of the CNT-FET.

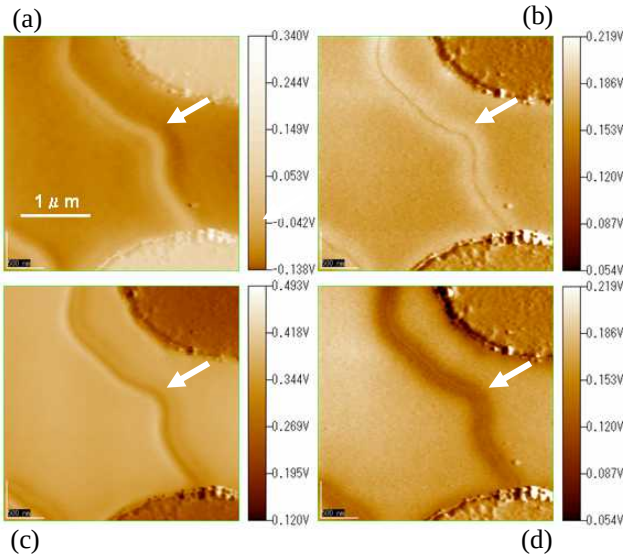

Fig. 3. Surface potential images of the CNT-FET at various V_{GS} conditions. (V_{DS}=-0.3 V)
(a) V_{GS} = -5 V.
(b) V_{GS} = 0 V just after -5 V gate bias stress.
(c) V_{GS} = +5 V.
(d) V_{GS} = 0 V just after +5 V gate bias stress.

It is notable that the potential in the area surrounding the CNT indicated by arrows is different from each other even though the gate bias voltage is same as 0 V as shown in Fig. 3(b) and 3(d), depending on the gate bias sequence; (b) from -5 V to 0 V and (d) from +5 V to 0 V.

In addition, the time dependent potential change was observed. Figure 4 shows the line profiles for various times after the gate bias stress at the position indicated by the bar in the inset of Figure 4. When the gate bias stress of -5 V was applied, the potential around the CNT showed decreasing tendency, as shown by the thick arrow in Fig. 4(a). On the other hand, when the gate bias stress of +5 V was applied, the potential around the CNT showed increasing tendency, as shown in Fig.4(b).

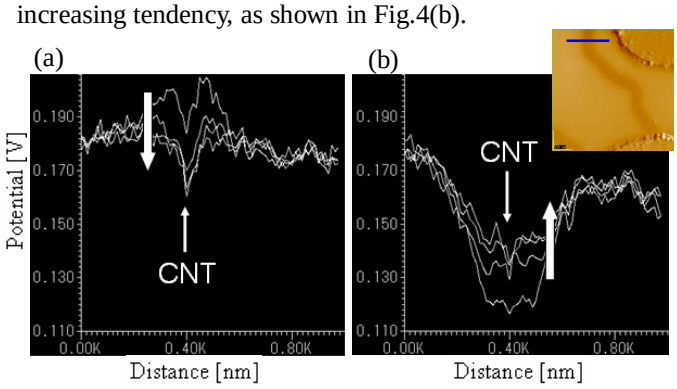

Fig. 4. Line profiles of the surface potential of the CNTFET.
(a) V_{GS} = 0 V just after -5 V gate bias stress.
(b) V_{GS} = 0 V just after +5 V gate bias stress.
(The bar in the inset indicates the position where the line profiles are shown.)

We have compared this result with the drain current (I_D) transient. Figure 5(a) and 5(b) show the transient of I_D (solid line) and the potential (dotted line) for the device after negative (-5 V, 60 s) and the positive (+5 V, 60 s) gate bias stresses, respectively. In the case of the negative gate bias stress, I_D was 0 A independent of time. In the case of the positive gate bias stress on the other hand, I_D showed decreasing transient. This behavior can be explained if we take into account the clockwise hysteresis of the I_D of the normally-off FET observed in the present device. When the negative gate bias stress is applied, no drain current should be observed as shown by the solid line in the inset of Fig.5. However, when the positive gate bias stress is applied, the I_D transient decreasing toward steady state value of 0 A should be observed, as shown by the thick white arrow in the inset. The dotted line in Fig. 5 (b) show the transient of the surface potential obtained in Fig. 4(b). The time constant of both I_D and the surface potential is almost same. This supports the above explanation in which the I_D transient and/or the hysteresis were caused by the surface potential change.

3. Summary

The surface potential of the CNT-FETs with small diameter channel was successfully measured by using the KFM. The time dependent surface potential was observed, which was consistent with the I_D transient and/or the hysteresis.

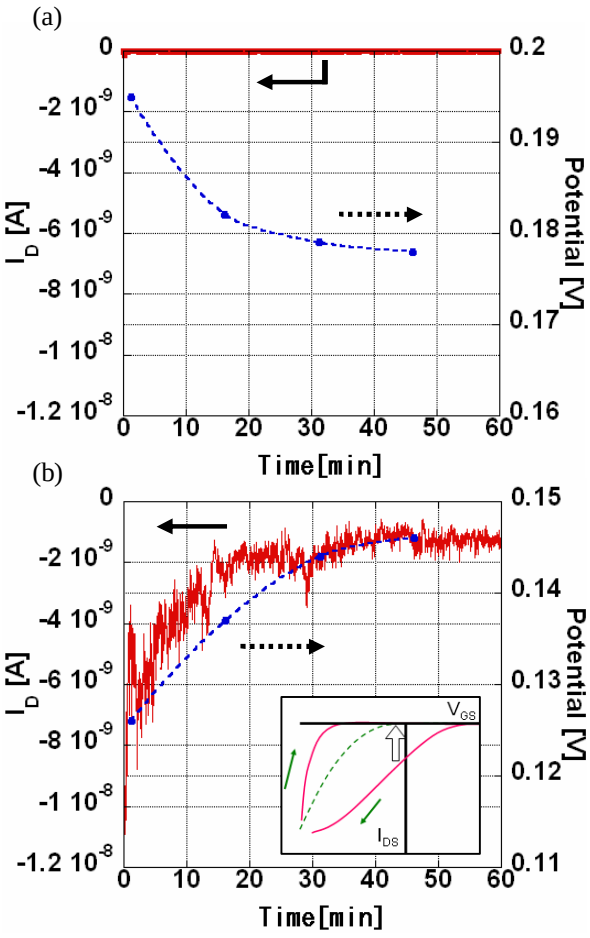

Fig. 5. Time dependent behaviors of the I_D and the surface potential.
(a) V_{GS} = 0 V just after -5 V gate bias stress.
(b) V_{GS} = 0 V just after +5 V gate bias stress.
Inset shows the schematic figure of the hysteresis.

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