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Semiconductor Nanowire Devices for Future Logic and Memory
(Invited Paper)

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1. Introduction

The demand for computing power and data storage capacity has been the driving force in the last 3~4 decades in semiconductor industry [1]. Fundamentally, the IC chip technology employs the *top-down* approach in which the devices and interconnects are made by processes such as lithography, thin-film, etching, and metallization. In addition to fabrication challenges, the top-down fabrication is facing three limits: i) scalability, ii) performance, and iii) power dissipation. First, the shrinkage of CMOS transistor geometry into nanometer scale is increasingly difficult due to leakages (gate tunneling, short-channel effects, band-to-band tunneling, etc.) that cause logic functionality failure. Second, Si is reaching its intrinsic speed limit. Alternative materials with higher carrier mobility, such as Ge or III-V compounds, regained great attention. To keep advancing semiconductor chip technology in performance, density, power control, and manufacturing cost reduction, new materials and technologies with *non-traditional* routes have to be sought after to meet the long-term roadmap demands.

2. Nanowire-Based Logic Computing

As shown in Fig. 1, the CMOS FET active region has been aggressively reduced from 3-D (bulk silicon) to 2-D (SOI) [2] and to 1-D (FinFET on SOI) [3], in order to gain adequate control over the electrostatics in an ultra-scaled MOSFET. One-dimensional semiconductor nanowires are among the smallest structures for effective transport of carriers. They may serve as both devices and interconnects. Synthesized by selected chemical methods, semiconductor nanowires have advantages such as scalable critical dimension made by non-lithographic assembly, ideal cross-section for ultra-scaled FET, and improved carrier transport due to reduced phonon scattering at low dimensionality.

Growth of 1-D anisotropic crystals (whiskers) was found in ore in 1500's. In 1970's, 1-D "microwires" were first synthesized in scientific laboratory. Only until 1990's, 1-D "nanowires" were made possible due to the rapid advancement in nanoscale fabrication and characterization techniques. The typical diameter of a lab-made nanowire ranges from a few to hundreds of nanometers with the length up to several tens of micrometers. In the last 5~6 years, varieties of semiconductor nanowire, including IV elements (Si, Ge) and III-V compounds (GaAs, InAs, InN, etc.), have been synthesized through different methods, e.g. vapor-liquid-solid (VLS), solid-phase diffusion & epitaxy, and solution-based reaction. Semiconductor nanowires are commonly made via metal-catalyzed VLS mechanism.

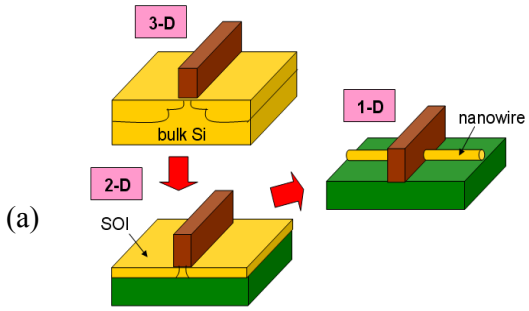

Fig. 1 Continued scaling of CMOS into deep-nanometer regime requires aggressively reduction of transistor physical geometry and dimensionality.

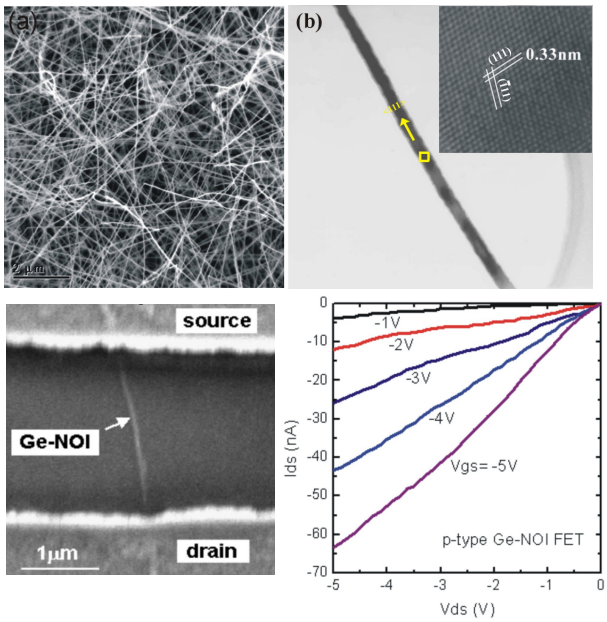

Fig. 2 (a) SEM image of as-synthesized germanium nanowires-on-insulator (Ge-NOI). (b) TEM image of Ge-NOI. (c) Fabricated Ge-NOI nanowire FET. (d) I-V characteristics (gate Tox ~30nm).

Various prototypes of circuit building block have been demonstrated including p-n junction, FET, logic gates and interconnect [4-7]. Though the mechanism of carrier transport/scattering in 1-D nanowire still lacks sufficient understanding, the best reported electron mobility in a Si nanowire FET is several times that of a planar bulk-Si FET,

likely due to reduced phonon scattering and effective surface passivation [7]. The lithography-independent cross-section, high carrier transport, and low synthesis cost make nanowire-FET good candidate for deeply extended CMOS, perhaps scalable down to a few nanometer gate length. Most attractively, the ease to synthesize high-transport nanowire on any substrate with extremely low cost is a big advantage. Fig. 2 shows the Ge nanowires-on-insulator (Ge-NOI) technology proposed in our lab [8], a concept similar to SOI technology. The Ge-NOI technology may offer low-cost integration for future logic IC chips. Prototype logic FET has been made with an I_{ON}-to-I_{OFF} current ratio of ~10^5 and an extremely low power.

3. Nanowire-Based Data Storage

For data storage application, programming efficiency and low-voltage/low-power operation may be achieved due to large surface-to-volume ratio of nanowire that offers large modulation of conductance under surface excitation. Fig. 3 shows schematically a memory device based on an array of vertical semiconductor nanowires. The footprint of the memory cell is very small due to the vertical cell structure. The large aspect ratio of nanowire also favors programming efficiency. In addition, the array architecture may help breaking the traditional limitation set by speed-density trade-off, potentially providing very low cost, high density, fast access and non-volatile data storage.

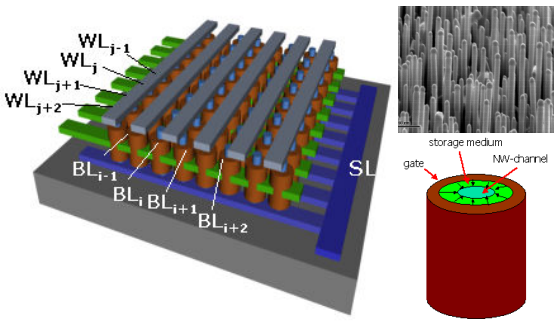

Fig. 3 Vertically assembled 1-D semiconductor nanowire array potentially used for ultrahigh-density fast-access memory chip.

In the so-called "hybrid integration" scenario, nanowire may be integrated with functional molecular components for data storage. Fig. 4a shows a nanowire memory cell with a monolayer of self-assembled molecules as data storage medium. Upon self-assembled on nanowire surface, the orbital structure of the molecule determines the behavior of charge transfer through the interface. Such a charge transfer process can be managed for nonvolatile data storage with retention time impacted by the molecular linker "tunneling barrier". Individual molecules in a self-assembled monolayer are used for charge storage. This allows high tolerance to molecular defect. Nanowire-based nonvolatile molecular memory has been demonstrated recently with multiple-level (up to 8-levels or 3-bits per cell) data storage and the best retention time up to one month has been observed [9].

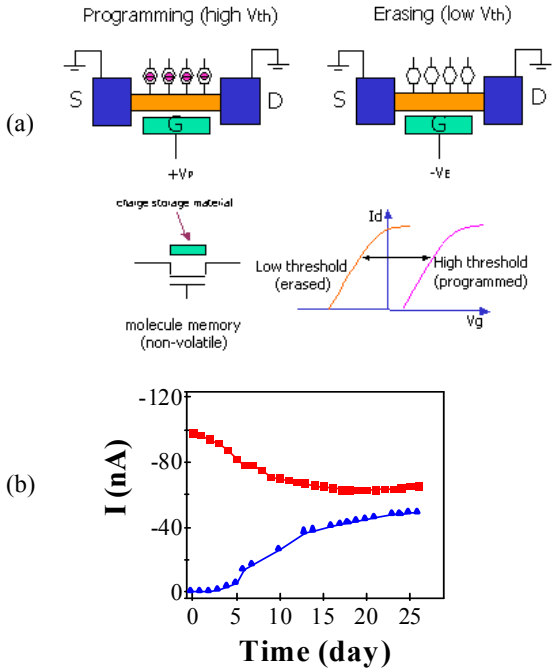

Fig. 4 (a) Semiconductor nanowire-based nonvolatile memory using self-assembled molecular monolayer for charge storage. The electrons tunnelling through the ultrathin linker "potential barrier" (~1nm) are stored in the molecular redox center (Fe). (b) Data retention curve of the fabricated molecular memory prototype.

4. Summary: Opportunity & Challenge

Due to their unique physical and electrical properties, one-dimensional semiconductor nanowires offer some great potentials in making future logic and memory devices with continuously improved performance, functionality, and density, possibly breaking the traditional scaling barrier via bottom-up nanomaterial synthesis and disruptive fabrication technologies, not through straightforward device geometry reduction. However, solid research progresses on controlled synthesis, integration compatibility with mainstream chip manufacturing environment, and demonstration of device prototypes with significantly enhanced performance and functionality would be among the greatest challenges.

References

[1] ITRS Roadmap, 2005 version.
[2] D. Hisamoto, *IEDM Tech. Dig*. (2001) 429
[3] B. Yu, et al, *IEDM Tech. Dig*. (2002) 937
[4] Y. Cui, et al, *Science* (2001) 291, 851
[5] Y. Huang, et al, *Science* (2001) 294, 1313
[6] N. A. Melosh, et al, *Science* (2003) 300, 112
[7] Y. Cui, et al, *Nano Lett*. (2003) 3, 149
[8] J. Yu, et al, *J. Phys Chem*. (2000) 104, 11864
[9] X. Duan, et al, *Nano Lett*. (2002) 2, 487
[10] N. A. Melosh, et al, *Science* (2003) 300, 112
[11] X. Duan, et al, *Nature* (2003) 425, 274
[12] M. C. McAlpine, et al, *Nano Lett*. (2003) 3, 1531
[13] S. V. Totkin, et al, *Appl. Phys. Lett*. (2003) 83, 1623
[14] B. Yu, et al, *IEEE Nano Conf*. (2005)
[15] C. Li, et al, *App. Phys. Lett*. (2004) 84, 949