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Charge Polarity Dependence of Negative Differential Conductance in Room-Temperature Operating Silicon Single-Charge Transistors

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1. Introduction

Silicon single-charge transistors (SCTs) are promising circuit elements that will add new functionalities to conventional VLSI. In order to achieve the integration of SCTs into VLSI, room temperature (RT) operation of SCTs is essential. Recently, large Coulomb blockade (CB) oscillations with large peak-to-valley current ratio (PVCR) have been observed at RT in silicon single-electron/hole transistors (SETs/SHTs) fabricated by high yield process [1-3]. Such SETs/SHTs have a large quantum level spacing in the ultra small silicon quantum dot, and negative differential conductance (NDC) can be observed at output characteristics [1-6]. NDC is expected to be a new operation mode of SETs/SHTs for highly functional circuit applications. However, NDC has been observed at RT in only SHTs [2,7].

In this study, we also observed clear NDC at RT in SETs fabricated by the same process as previously reported SHTs and compared NDC in SET and SHT for the first time. Considering this result, the physical origin of appearance of NDC was discussed.

2. Experiments and Results

In order to investigate the possibility of NDC appearance in SETs, we fabricated n-type and p-type common wire channel MOSFETs [7] as shown in Fig. 1(a). Thanks to this common channel structure, transport property of electron/hole can be studied in the same physical channel profile. Fig. 1(b) and (c) show the upper SEM image and the cross sectional TEM image of the ultra narrow channel. Fig. 1(c) indicates the formation of gate-all-around (GAA) structure. Fig. 2 shows drain current (I_d) versus gate voltage (V_g) characteristics at RT, where large CB oscillations are observed not only in SHT but in SET. This indicates that ultra small silicon dot can be formed in an n-type channel as well.

Then, SETs are fabricated in the form of ultra narrow channel MOSFET with optimized process. Figs. 3 and 4 show I_d-V_g characteristics and I_d versus drain voltage (V_{ds}) characteristics in a fabricated SET, respectively. From this result, we have observed clear NDC in SET. Fig. 5 shows the Coulomb diagram in this SET, in which extended CB region appears in the negative V_{ds} region. Figs. 6, 7, and 8 show I_d-V_g characteristics, I_d-V_{ds} characteristics, and Coulomb diagram in another fabricated SET, respectively. Figs. 9 and 10 show I_d-V_g characteristics and I_d-V_{ds} characteristics in a fabricated SHT. From this result, we have observed clear NDC in SHT. Fig. 11 shows the Coulomb diagram in this SHT, in which extended CB region appears in the positive V_{ds} region.

3. Discussion on Physical Origin of NDC appearance

In a SET (Fig. 8) the extended CB region due to large quantum confinement appear at negative V_{ds}, while it appears at positive V_{ds} in a SHT (Fig. 11). This means that the extended CB region appears when the drain Fermi level energy (E_F) is pulled up for both electron and hole. This can be explained in terms of electrical capacitive coupling between silicon dot and drain [5]. In the previous report, coupling capacitance to source and drain, C_s and C_d, is expected to be small in the narrow channel structure [5].

Especially in our fabricated 200-nm-long ultra narrow channel SET/SHT, C_s and C_d becomes small due to GAA structure. Actually, because of this small C_s and C_d, the slope of the boundary in CB region with drain E_F pulled down, $-C_g/C_d$, becomes very steep, and that with drain E_F pulled up, C_g/C_g+C_s, becomes nearly unity.

Fig. 12 shows an equivalent circuit of a SET, band diagram, and boundary of Coulomb diagram. Small C_d leads to large voltage drop at the drain side tunneling junction. NDC is considered to be mainly due to large quantum level spacing and the decrease of tunneling probability at carrier injection side as quantum level is pulled down [2]. With drain E_F pulled down, voltage drop at the source side junction is small and the decrease of tunneling probability becomes small. Therefore, NDC does not tend to appear. On the other hand, with drain E_F pulled up, voltage drop at the drain side junction is large and the decrease of tunneling probability becomes large. Therefore, NDC tends to appear.

Considering above discussions, the tunneling condition at drain side largely may affect NDC appearance in ultranarrow channel SET. In order to examine the effect of the tunneling condition, the Coulomb diagram in Fig. 5 is measured again by exchanging source and drain of the SET, as shown in Fig. 13, in which the extended CB region does not appear. If we assume symmetric tunneling barriers, NDC should appear even by exchanging source and drain. This phenomenon can be explained by asymmetric tunneling barriers. Band diagrams of Fig. 6 and Fig. 14 correspond to Fig. 14 (a) and (b), respectively. In Fig. 14 (a), the tunneling barrier curvature at the drain side is small and the decrease in tunneling probability is large. Therefore, NDC tends to appear. On the other hand, in Fig. 14 (b), NDC does not tend to appear.

4. Summary

We observed clear NDC at RT in SET fabricated by the same process as previous SHTs and compared NDC in SET and that in SHT. In addition to large quantum level spacing and tunneling barrier structure, electrical coupling condition is critical factor for NDC appearance.

References

[1] K. Uchida et al., *IEDM*, p.863, 2000. [2] M. Saitoh et al., *IEDM*, p.753, 2003. [3] M. Saitoh et al., *IEDM*, p.187, 2004. [4] H. Ishikuro et al., *Appl. Phys. Lett*., 71, 3691, 1997. [5] Y. Ono et al., *Jpn. J. Appl. Phys*., 41, 2569, 2002. [6] M. Saitoh et al., *Jpn. J. Appl. Phys*., 43, L210, 2004. [7] K. Miyaji et al., *SSDM*, p.166, 2005 [8] H. Ishikuro et al., *IEDM*, p.119, 1998.

Acknowledgment

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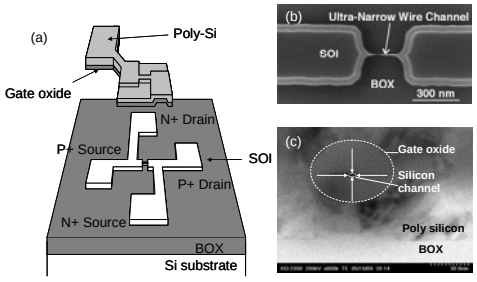

Fig. 1 (a) Schematic of an n/p common wire channel MOSFET. (b) A SEM image. (c) A cross sectional TEM image of an ultra narrow channel.

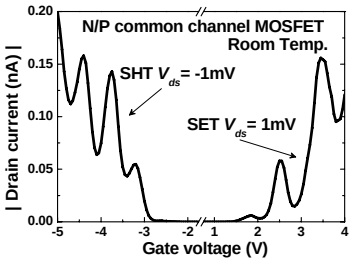

Fig. 2 Measured I_d-V_g characteristics in an n/p common wire channel MOSFET at RT.

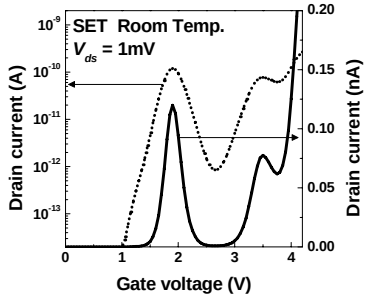

Fig. 3 Measured I_d-V_g characteristics in an ultra narrow wire channel SET.

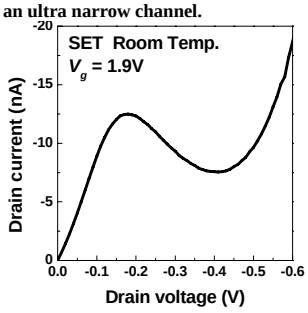

Fig. 4 Measured I_d-V_{ds} characteristics in an ultra narrow channel SET.

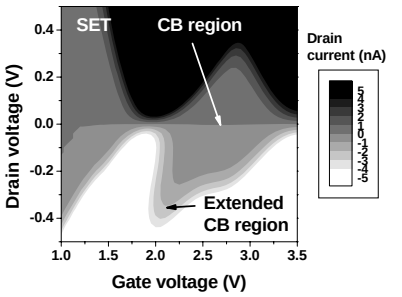

Fig. 5 Measured contour plot of I_d as a function of V_g and V_{ds} in an ultra narrow channel SET.

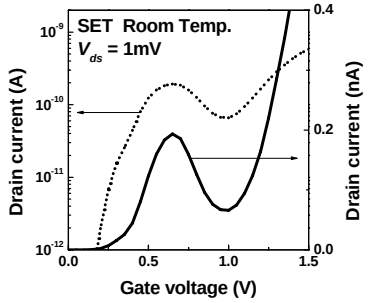

Fig. 6 Measured I_d-V_g characteristics in an ultra narrow wire channel SET.

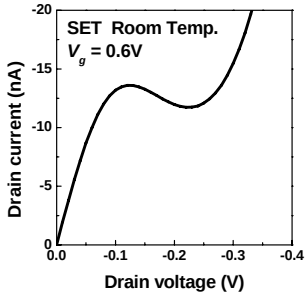

Fig. 7 Measured I_d-V_{ds} characteristics in an ultra narrow channel SET.

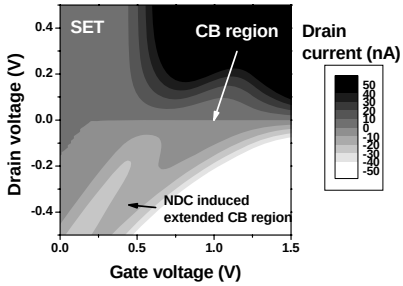

Fig. 8 Measured contour plot of I_d as a function of V_g and V_{ds} in an ultra narrow channel SET.

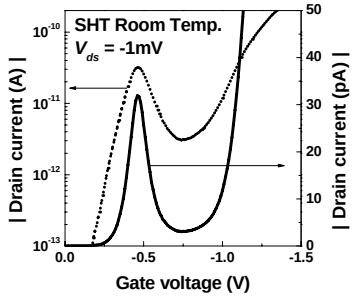

Fig. 9 Measured I_d-V_g characteristics in an ultra narrow wire channel SHT.

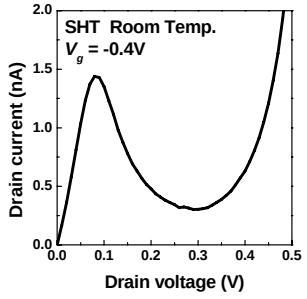

Fig. 10 Measured I_d-V_{ds} characteristics in an ultra narrow channel SET.

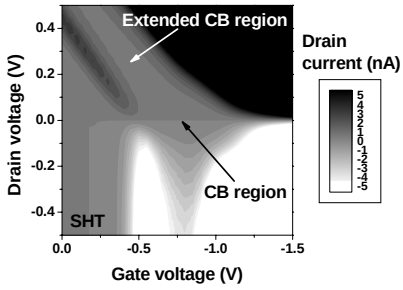

Fig. 11 Measured contour plot of I_d as a function of V_g and V_{ds} in an ultra narrow channel SET.

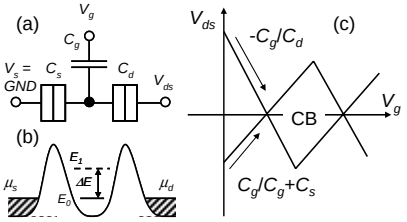

Fig. 12 (a) An equivalent circuit of a SET. (b) A schematic of the band diagram. (c) A schematic of the boundary of a CB region.

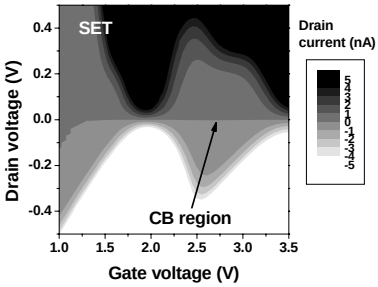

Fig. 13 contour plot of SET in Fig. 5 is measured again by exchanging source and drain.

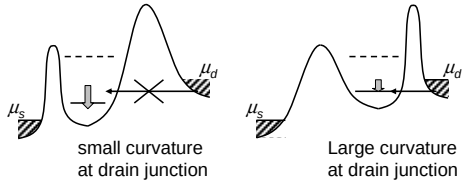

Fig. 14 Band diagrams of SETs with asymmetric tunneling barriers. (a) NDC tends to appear. (b) NDC does not tend to appear.