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High-PVCR Si/Si_{1-x}Ge_x Planer-Type Resonant Tunneling Diode Formed with Phosphorous doped Quadruple-layer Buffer

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1. Introduction

Si/Si_{1-x}Ge_x resonant tunneling diodes (RTDs) have been intensively studied as one of next-generation quantum effect devices formed with Si-system materials. The *I-V* curves show negative-differential-resistance (NDR) characteristics. In the practical level, peak-to-valley current ratios (PVCRs) of $> \sim 10$ and current densities of $> \sim 10 \text{ kAcm}^{-2}$ are required for the high frequency operation at room temperature (RT).

Previously, we have applied a combination of electron tunneling and multiple wells using the type II band offset, and have reported high PVCRs of 8 - 180 at RT [1,2]. To form the type II hetero structure, a strain-relaxed SiGe buffer should be formed on the Si substrate.

For the SiGe buffer, we have proposed a triple-SiGe-layer (TL) buffer and have experimentally cleared the relaxation mechanisms as shown in Fig. 1 [3]. In the TL buffer formation process, the 1st and 2nd layers are grown coherently. The top 3rd layer relaxes the lower SiGe layer and prevents threading dislocations from being propagated to the top buffer surface. The top layer relaxation rate reaches 50%.

However, high phosphorous (P) doping in the TL buffer, to increase the RTD current density, degrades the surface crystallinity due to the potential fluctuation induced by P dopants during the layer growth and the threading dislocations are easily generated. To solve this problem, we have proposed a quadruple-SiGe-layer (QL) buffer where misfit dislocations are evenly distributed in the lower two interfaces and a higher crystalline buffer surface is obtained.

It is also considered that electron trap at the misfit dislocation center degrades the *I-V* reproducibility. Thus, we have first applied the doped QL buffer with a better crystalline surface to an electron tunneling RTD and have further applied a planer-type device structure to the RTD, where the

electrons can flow without passing through the misfit dislocation interfaces of the QL buffer for trapping at the misfit dislocation defects. As a result, we have obtained an electron-tunneling Si/SiGe RTD exhibiting better NDR reproducibility with high PVCR and high current density at RT.

2. Experimental

Si and Si_{1-x}Ge_x layers were grown on 2-3 Ωcm n-type Si(001) at a substrate temperature of 600 °C by gas-source molecular beam epitaxy in an ultra-high-vacuum compatible chamber with a base pressure of $< 1 \times 10^{-9}$ Torr using Si₂H₆, GeH₄ and PH₃ for Si, Ge, and dopant gas sources, respectively.

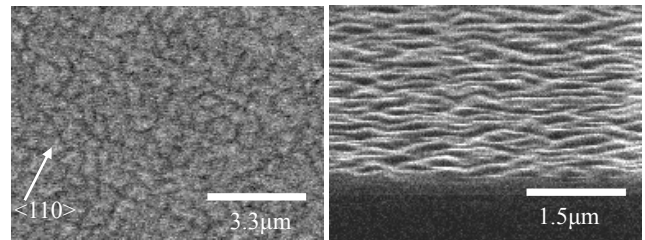


Fig. 2. Top view (left) and bird's-eye view (right) of the doped TL buffer.

3. Results and Discussion

3.1 Doped quadruple-layer (QL) buffer technology

First, we carried out P doping for our previously proposed TL buffer [3]. The doping density was $2 \times 10^{19} \text{ cm}^{-3}$. The relaxation rate of the top layer of the TL buffer was as low as 28 %, however, the cross-hatched lines generated by 60° dislocations were observed in the $\langle 110 \rangle$ directions with a 400 nm line space as shown in Fig. 2. Typical SEM image also shows large surface roughness (the right photo of Fig. 2). Thus, the TL buffer surface is degraded by high P doping.

Designed and fabricated P-doped QL buffer is shown in Fig. 3. Typical SEM images and RHEED pattern of the QL buffer surface are shown in Fig. 4. The doping density was $2 \times 10^{19} \text{ cm}^{-3}$. Although the relaxation rate of the 3rd Si_{0.75}Ge_{0.25} layer reached 62%, cross-hatched lines were very weak and the surface was very flat (Fig. 3(a)). The RHEED pattern were also streaky (Fig. 3(b)), indicating that the surface local flatness is on the level of an atomic layer.

As for the TL buffer, the lattice mismatch analyses indicate that the misfit dislocations are concentrated in the lower interface [3]. On the other hand, the measured lattice mismatches of the QL buffer are also indicated in Fig. 3. The

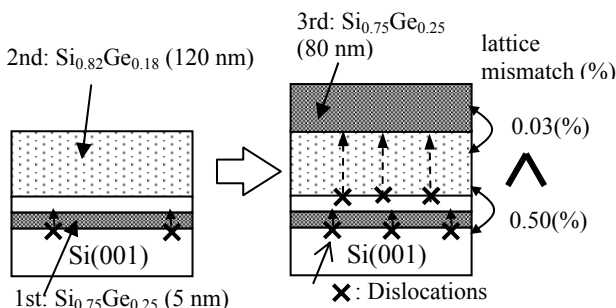


Fig. 1. Relaxation mechanisms of our previously proposed triple-SiGe-layer buffer.

lattice mismatches are large between the Si substrate and the 1st layer and between the 1st and 3rd layers and they are almost the same. Thus, dislocations are distributed almost evenly in the lower two interfaces and the generation of threading dislocations in the two top layers are effectively restrained. The generation of threading dislocations in the two top layers is effectively restrained. Thus, due to the even dislocation distribution in the two lower interfaces, the high surface crystallinity is also obtained even under high P doping during the buffer growth.

It is estimated that Si on the QL buffer is strained by 0.93 % and this Si strain rate corresponds to the strain of Si on fully relaxed $\text{Si}_{0.84}\text{Ge}_{0.16}$. The strain also corresponds to that of a 1.6 μm graded buffer [4]. The graded buffer thickness is seven times larger than that of the QL buffer.

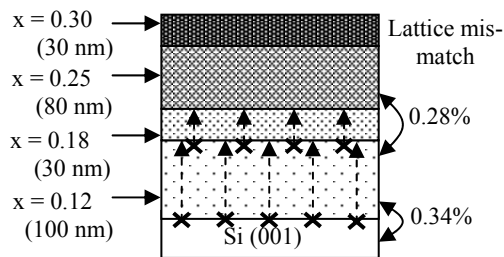
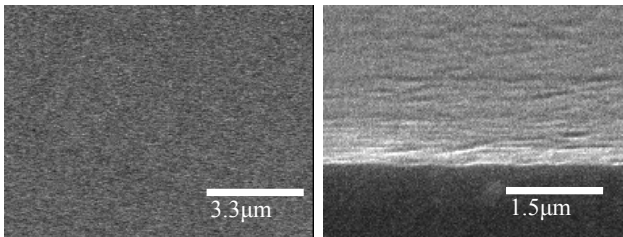
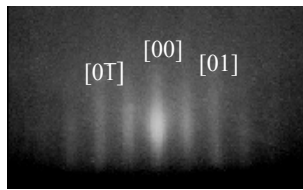


Fig. 3. Structure of the QL buffer doped with P and obtained lattice mismatches.



(a) Top view (left) and bird's-eye view (right) of the QL buffer



(b) RHEED pattern

Fig. 4. Typical SEM and RHEED images of the doped QL buffer.

3.2 Static performance of a planer-type RTD formed with the QL buffer

We fabricated Si/SiGe RTDs using the doped QL buffer. On the buffer layer, double well structure (5 nm strained Si well / 1.5 nm unstrained $\text{Si}_{0.70}\text{Ge}_{0.30}$ barrier) and collector region (30 nm $\text{n-Si}_{0.75}\text{Ge}_{0.25}$ / 15 nm n-Si / 15 nm i-Si) were grown. Barrier height was about 80 meV estimated from the relaxation rate of the $\text{Si}_{0.75}\text{Ge}_{0.25}$ layer. To prevent the electron current from passing through dislocation defects in the interfaces of the buffer, we designed a planer-type RTD structure which is illustrated in Fig. 5. The well region is cylinder shaped and the diameter is 20 μm . The typical I - V curve obtained from the RTD at RT is shown in Fig. 6. The

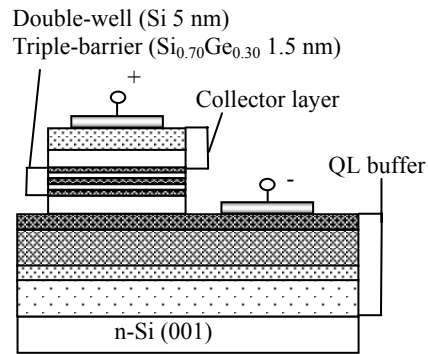


Fig. 5. Structure of a planer-type RTD fabricated with the P-doped OL buffer.

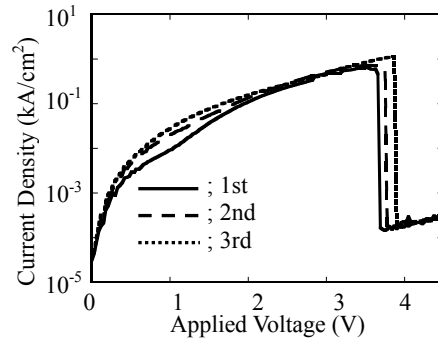


Fig. 6. Typical I - V characteristics of a planer-type RTD fabricated with the P-doped QL buffer.

planer-type RTD exhibits well NDR reproducibility with high current density of the order of kA/cm^2 and high PVCr.

4. Conclusion

We have proposed a quadruple-layer (QL) buffer on the basis of the strain-relief mechanisms of the TL buffer. The QL buffer has been confirmed to have well crystallinity by SEM image and RHEED pattern observations. To analyze the lattice mismatch, the misfit dislocations are evenly distributed in the lower two interfaces leading a high crystalline buffer surface even if the buffer is grown under high P doping. Using a combination of a highly doped QL buffer and a planer structure, we have obtained an electron tunneling Si/SiGe RTD exhibiting well NDR reproducibility with high PVCr and high current density.

Acknowledgements

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