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Tunnel-coupled double nanocrystalline Si quantum dots integrated into a single-electron transistor

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1. Introduction

Recently the double quantum dot (DQD) structure has been studied as a charge qubit to realize the solid-state quantum computer. DQDs have first been fabricated in GaAs:AlGaAs heterostructures, where DQDs are realized through the depletion of a two-dimensional electron gas using surface gates[1]. DQDs have also been fabricated in the Si-based materials by using the electron beam lithography and the reactive ion etching (RIE) techniques, which results in a ‘‘trench-isolated’’ structure [2]. Charge polarization in the DQDs is measured using a quantum point contact (QPC) or a single-electron transistor (SET).

To realize the practical quantum computer, computation steps (=decoherence time/coherent oscillation period) must be increased at least by 10^4 times. To meet this computational requirement, increasing the decoherence time and the coherent oscillation frequency is the necessary condition. One of the solutions is using the smaller sized quantum dots (QDs) which show larger quantum effects. In the present work, we succeeded in integrating the lithographically patterned SET and nanocrystalline-Si (nc-Si) dots. Average diameter of the nc-Si dots is approximately 10nm, and they are deposited using the UHV-PECVD system. These nc-Si dots are single crystalline and highly pure in nature. These unique properties will help to realize the long decoherence time charge qubits. We carried out the differential current measurement to estimate the coupling capacitance values. To investigate the effects of the existence of nc-Si QDs and their charge polarization on the SET characteristics, we performed an equivalent circuit simulation.

2. SET Fabrication

We fabricated a single dot structured SET on silicon-on-insulator (SOI) with four side gates. The schematic top-view of the SET is shown in Fig. 1(a). The colored regions indicate Si (P doped $\sim 10^{19}$ cm^{-3}) and the white regions indicate the buried-oxide layer (BOX) of the SOI material, where the Si has been etched away using the electron cyclotron resonance RIE (ECR-RIE) technique. The thickness of the doped Si layer and the BOX layer are 40 nm and 200 nm, respectively. The SET was patterned using the high-resolution electron beam lithography with a lithographically defined diameter of approximately 90 nm for the island. The adjacent constrictions, that act as tunnel barriers connecting the charging island to the source and drain leads are of 70 nm in width. The pattern was etched using the ECR-RIE technique and was thermally oxidized at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI down to 30 nm. This leads to the resulting overall dot diameter of approximately 70 nm.

3. SET measurement

Electrical measurements were carried out at the temperature of 4.2 K, for the device operating in the Coulomb blockade regime with the drain to source bias voltage of 1mV. The gate bias dependence of the device obtained by sweeping the voltage V_{G4} at the different values of V_{G2} is shown in the Fig. 1(b). It depicts the measured differential current $\partial I_D / \partial V_{G4}$. Coupling capacitances between the gates G4 and G2 and the SET island are estimated from the differential current characteristics C_{G4}=1.1 aF, C_{G2}=1.6 aF, respectively. The total capacitance is estimated to be $C_\Sigma \approx$16 aF from the Coulomb gap voltage $V_{gap} \approx$ 10mV.

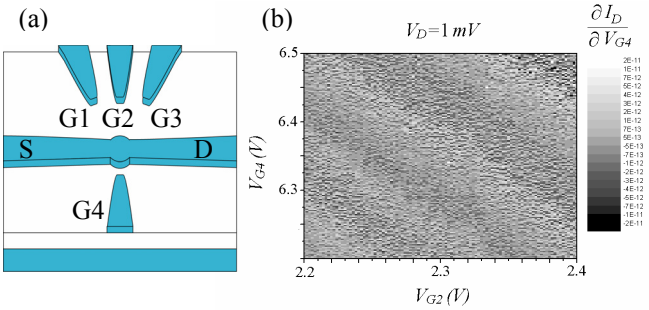

Fig.1 (a) Schematic top-view of the lithographically fabricated single dot structured SET with four gates. (b) The gate dependence of the conductance $\partial I_D / \partial V_{G4}$, obtained through sweeping the voltage V_{G4} at different values of V_{G2}.

4. Integration of nc-Si QDs with the SET

Integration of size-controlled nc-Si QDs with the SET was done by using our UHV-PECVD nc-Si deposition technique. After fabricating the SET, a resist hole was prepared in the narrow region between the SET island and 3 gate electrodes (G1, G2, and G3) using the electron beam lithography. After that nc-Si dots were deposited on the SET patterned substrate. The nc-Si QDs therefore contacted directly to the substrate only in the resist hole area. Fig. 2 describes the fabrication processes involved in integrating nc-Si QDs and the SET in detail. As last, the resist is

removed from the substrate (Fig.3 (a)).

5. Equivalent circuit simulation

To study the effects of the existence of nc-Si QDs and their charge polarizations on the SET electrical characteristics we carried out the equivalent circuit simulation. The equivalent circuit of the SET with nc-Si QDs is shown in Fig. 3 (b). Figure 4(a) shows the simulated gate dependence of $\partial I_D / \partial V_{G4}$ done as a reference without the nc-Si dots. Figs. 4(b), (c) and (d) show the results for various charge configurations of nc-Si dots. These results indicate that nc-Si QDs help to shift the Coulomb oscillation peak lines effectively, and charge polarization with the magnitude of only $\pm e$ can be sensed as thier remarkable shift.

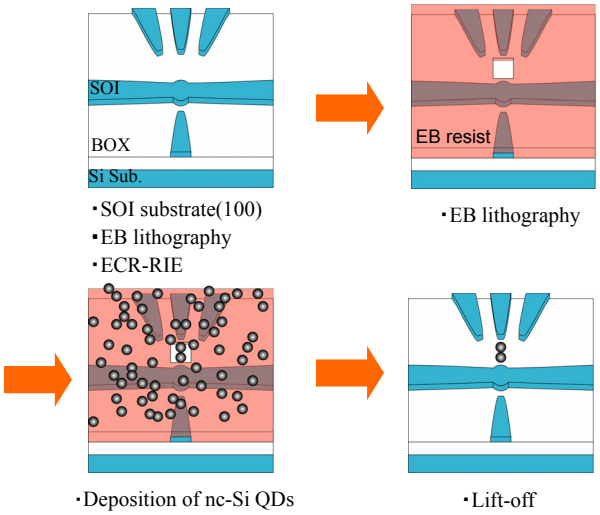

Fig.2 Fabrication processes involved in integrating the SET and nc-Si QDs.

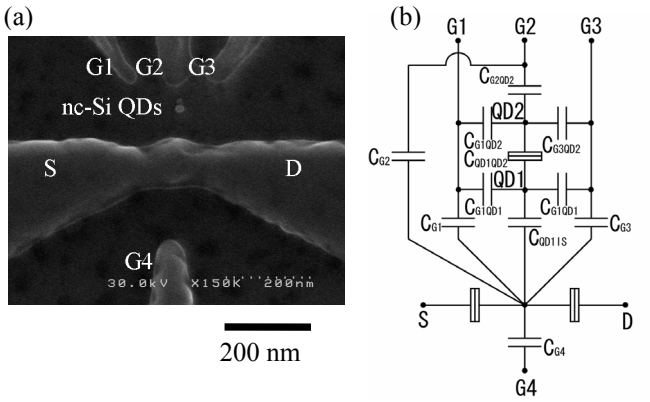

Fig. 3(a) SEM image of the nc-Si QDs integrated SET. (b) The simplified equivalent circuit of the device shown in Fig. 3(a). The simulations include the capacitance between G2 and QD1, and the capacitance between QD2 and the SET island.

6. Conclusion

The multi-gate SET was fabricated on the SOI, and the tunnel-coupled nc-Si DQDs were integrated into the SET for the first time. The equivalent circuit analysis showed that only $\pm e$ charge polarization can be sensed as a shift of the Coulomb oscillation peaks.

References

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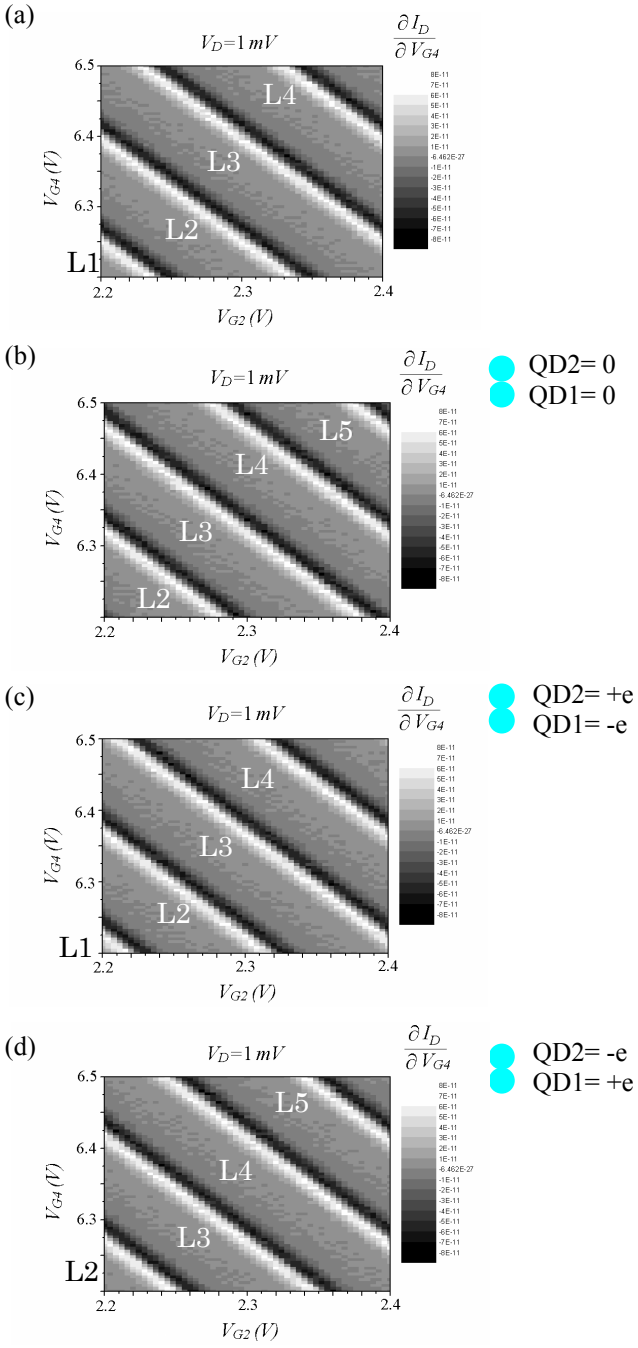

Fig. 4 (a) The characteristic of the SET without nc-Si QDs. (b) The characteristic of the SET with no charge polarization. (c), (d) the characteristics of the SET with charge polarizations shown in inset figures.