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Fabrication of Ge Quantum-dots by Oxidation of $Si_{1-x}Ge_x$-on-insulator Nanowires and its Applications to Resonant Tunneling Diodes and Single-electron/Single-hole Transistors

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1. Introductions

It is well known that quantum-dot (QD) structure is promising for single-electron and optoelectronic devices application due to the substantial quantum mechanics and confinement effects. The criteria for a successful and practical single-electron transistor is to make a nanometer scale QD (<10 nm) weakly coupled to source/drain electrodes via thin tunneling barriers. Different approaches have been reported for forming Si-based QDs, however, they might suffer from the issues of controllability, reliability, and compatibility with the conventional Si process technology. Recently, we have developed a simple and CMOS compatible method, selective oxidation of single crystalline $Si_{1-x}Ge_x$-on-insulator (SGOI), to form Ge QDs embedded in a SiO_2 matrix. During high temperature oxidation, Si is preferentially oxidized while Ge atoms are rejected out from the growing oxide. The segregated Ge atoms would diffuse and agglomerate to form Ge QDs. The average dot size and spatial density could be modulated by oxidation time and temperature as well as Ge content in the SiGe layer. In this paper, we reported that the Ge dot size and spatial density are also dependent on the patterns and geometry of SGOI before thermal oxidation. Using this technique, Ge-QD resonant tunneling diodes (RTDs) and single-electron/single-hole transistors (SETs/SHTs) with large peak-to-valley current ratio oscillations are experimentally demonstrated.

2. Experiments

The fabrication of Ge QDs and its related devices started from a silicon-on-insulator wafer with the top silicon layer and buried oxide layer thickness of 35 nm and 380 nm, respectively. A trilayer of a 10 nm Si buffer layer/an 8 nm strained $Si_{0.9}Ge_{0.1}$/a topmost 2 nm Si cap layer was grown by ultrahigh vacuum chemical vapor deposition at 550 ^oC. Then, SiGe/Si nanowires connecting source/drain (S/D) electrodes was patterned using electron beam lithography and SF_6/C_4F_8 plasma etching. The width of the nanowires varies from 25 nm to 70 nm. Subsequently, thermal oxidation was performed in H_2/O_2 ambient at 900 ^oC to completely oxidize the SiGe/Si nanowires from the top plane and sidewalls, which would induce the formation of Ge QDs embedded between the growing oxide and the buried oxide due to Ge atom segregation and agglomeration. Since the nanowire's width is less than its thickness, the required oxidation time for completely oxidizing the SiGe/Si nanowire is determined by the former. While only a small portion of SiGe/Si layer in the electrodes would be consumed once the nanowire is completely oxidized. The average QD diameter is 8.9±2.5 nm with the separation of 40 nm. For RTDs or SETs, after thermal oxidation, gate and S/D electrodes were implanted with 5×10^{15} cm^{-3} arsenic ions and then activated at 900 ^oC for 20 seconds. Finally gate, passivation, contact-hole patterning, metallization, and 400 ^oC forming gas sintering steps were performed to complete device fabrication.

3. Formation of Ge QDs: Pattern and geometry dependence

Figure 1 shows the plane-view transmission electron microscopy (TEM) images of Ge QDs formed by thermal oxidation of different geometric patterns; sample A is a big square with 100 × 100 μm^2 and sample B is a nanowire with the width of 40 nm and the length of 1 μm. Oxidation is performed mainly from the top plane for sample A, consequently, plenty of room or space allows for Ge diffusion and agglomeration, leading to the uniform distribution of Ge QDs with a small dot size of 3±1 nm and high spatial density of $1.2x10^{12}$ cm^{-2}, as shown in Fig. 1(a). On the contrast, the nanowire on sample B was oxidized not only from the top plane but also from the sidewalls simultaneously, which would induce the Ge diffusion confined by the growing oxide and consequently, larger Ge QDs are squeezed to the center of the oxidized nanowire. The average dot size and separation between two adjacent dots are 8.9±2.5 nm and 40 nm, respectively, as shown in Fig. 1(b). It is noted that the squeezed points near the ends of the nanowire prohibit the presence of Ge QDs due to the faster oxidation rate and limited space for Ge diffusion/agglomeration. This would naturally form the self-aligned tunneling barriers for RTD and SET applications.

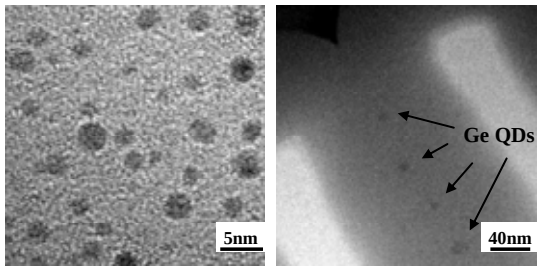

Fig. 1 TEM plane-view images of Ge QDs formed by thermal oxidation of (a) sample A: a 100 × 100 μm^2 square and (b) sample B: a 40 nm nanowire.

4-1. Ge-QD RTDs

Figure 2 shows the fabricated Ge-QD RTD with the Ge QDs formed by thermal oxidation of a 25 nm nanowire. The time-averaged current-voltage (I-V) characteristics of a Ge-QD/SiO_2 RTD with and without photoexcitation at room temperature are plotted in Fig. 3. For the Ge-QD RTD operating in the dark, the tunneling current displays a quasi-oscillatory behavior with a nearly periodic voltage separation of 0.15 V. Electrons are allowed to tunnel into the Ge-QD as the applied voltage exceeds the threshold voltage, 0.8 V, which corresponds to the filling of the ground state (E_e). The entrance of additional electron into the QD would be forbidden unless it gains enough energy to overcome the Coulomb repulsion from electron-electron interaction at the ground state. Under optical pumping, appealing features such as fine structures in the first current peak at voltage less than 0.8 V and enhanced negative differential conductance (NDC) are observed. It has been theoretically predicted that new tunneling current peaks would appear for a SET under photoexcitation due to the creation of excess holes in the QD. When electron-hole pairs are generated in the QD due to photoexcition in addition to the tunneling electrons, various exciton complexes such as the exciton, positive and negative trions, and biexciton can be formed. This would generate fine structures for the electrons to tunnel from the source to the drain electrode at voltage less than threshold voltage. Besides, the Ge-QD RTD displays a bistable current near the first peak as the applied voltage is swept in a loop as shown in the insert of Fig. 3.

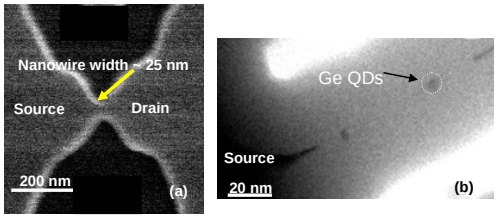

Fig. 2 Plane-view (a) scanning electron microscopy and (b) transmission electron microscopy image of Ge QDs formed by thermal oxidation of SiGe/Si-on-insulator nanaowires.

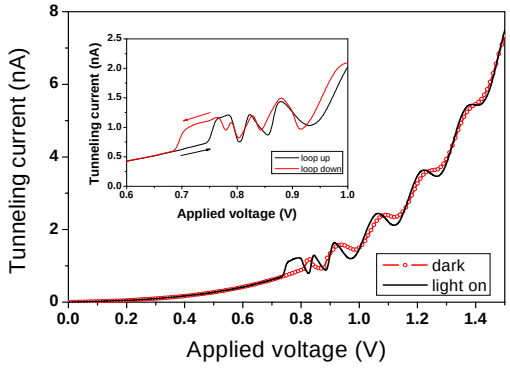

Fig.3 I-V characteristics of a Ge-QD/SiO_2 RTD at room temperature.

4-2. Ge-QD SETs/SHTs

Figure 4 reports the steady-state tunneling currents of a Ge-QD SET and SHT measured at room temperature. The nonperiodic Coulomb oscillation of tunneling current for SETs is due to the combination of multivalley effect, directional-dependent effective mass and asymmetrical shape of a QD. On the other hand, the resonant current of Ge-SHTs might provide useful information on the electronic structure of Ge QDs due to its single valley and isotropic effective mass. It is noted that the tunneling current of a Ge-SHT displays homogeneity of peak separation (ΔV_g = 0.43 V) and the resonant structures of a QD are clearly invariant with temperature. The current peaks in the curve at 250 K are one to one corresponding to those at 300 K. These thermal stable resonant structures indicate that the observed current should go through the energy levels of a Ge QD, but not through trap states. The single-hole addition energy, E_a, is estimated to be 43 meV from the drain current contour plot, which is close to 35 meV calculated using the k · p method.

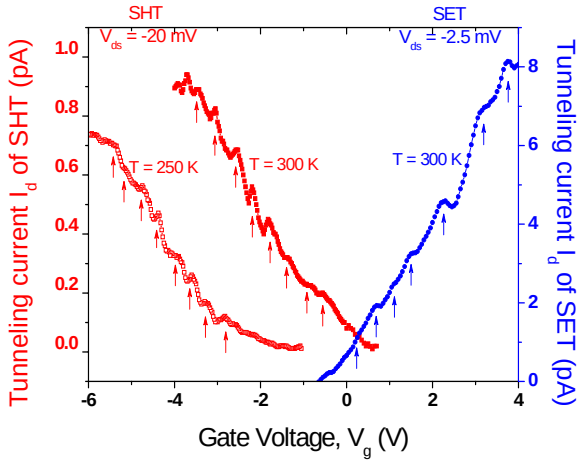

Fig. 4(a) Tunneling currents of a Ge-SHT and SET as a function of gate voltage at 300 K. (b) Tunneling currents of a Ge-SHT as a function of V_g at 300 K and 250 K, respectively.

5. Conclusions

We have reported a CMOS-compatible method for forming Ge QDs using thermal oxidation of SGOI nanoires. The impacts of geometry and patterns of SGOI on the Ge QD size and density are investigated. Using this technique, room-temperature Ge-QD RTDs and SETs/SHTs have been implemented with large peak-to-valley current ratio oscillations.

Acknowledgements

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