Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 822-823

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SET-based Flexible Multi-valued NAND and NOR Gates for Half-Adder

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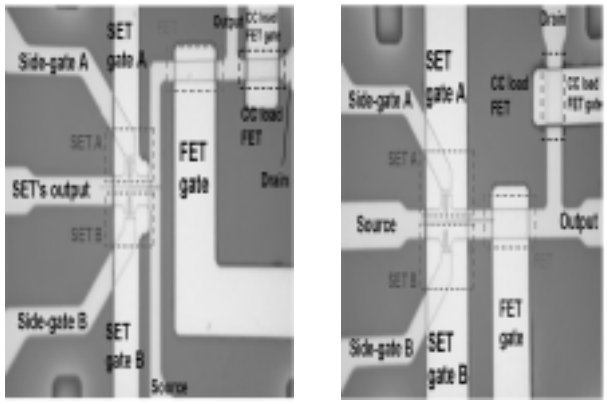
1. Introduction

Multiple switching on/off of a single-electron transistor (SET) enables us to realize the multiple-valued(MV) single-electron logic, which has higher functionality with low-power. A SET-based MV half adder needs a NAND (or NOR) and a XOR gate as essential device elements[1]. Here we report on a successful fabrication of Si SET-based flexible multi-valued NAND & NOR gate on a SOI chip. Their input-output voltage transfer characteristics display typical NAND or NOR gate functions for various binary or multi-valued two SET input voltages.

2. Device Structure and Fabrication Process

Incorporating SETs with FET, in-plane side gate-controlled NAND- and NOR-type gates were fabricated on a SOI chip. The resulting SET/FET circuit comprises of two identical SETs connected in series (parallel) (for the NAND (NOR)), a MOSFET and a constant-current load, which is seen in Fig. 1 with its corresponding circuit layout. In the SET part, Coulomb island and a side-gate were both defined in the same plane as the active channel by e-beam lithography and formed by deeply etching into the buried oxide. Such an in-plane structure is very efficient in Si fabrication process and the side gate adjacent to the Coulomb island channel of 20x50nm formed by pattern-dependent oxidation (PADOX) could easily control the phase of Coulomb oscillations of each SET, which enables to achieve the flexible multi-functionality of the voltage output of the circuit.

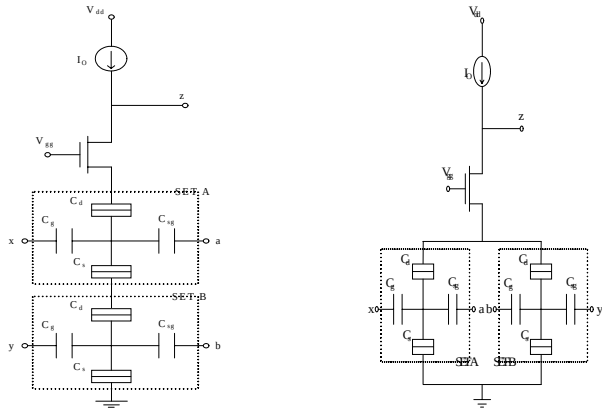


b)

Figure 1. (a) Schematic of the NAND & NOR logic gate circuit comprising of a MOSFET and two identical SETs which are connected in series, and in parallel, respectively. (b) SEM image of the resulting SET/FET NAND & NOR gates fabricated on a SOI chip.

3. Results and Discussions

Figure 2(a) & 3(a) are 3-D and a grayscale contour plot of the voltage output V_{OUT} as a function of two SET input voltages of Vin1 and Vin2 for NAND and NOR gates. The CC load current is set to 100pA with a voltage limit of 20mV and the V_{FET} is set to 841mV. The output circuit voltage V_{OUT} displays alternating high/low behavior as a function of two SET input voltages. The periodic high/low feature in V_{OUT}, exploited to multi-valued NAND and NOR gate functions, corresponds



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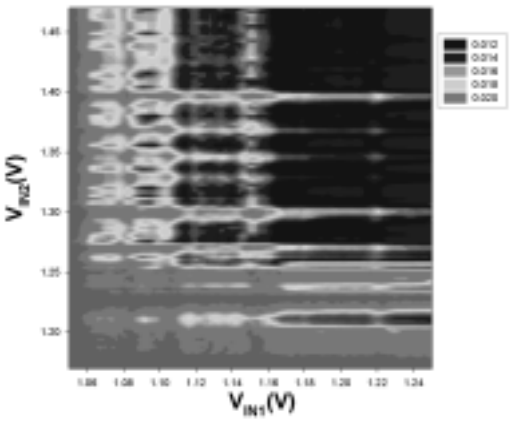

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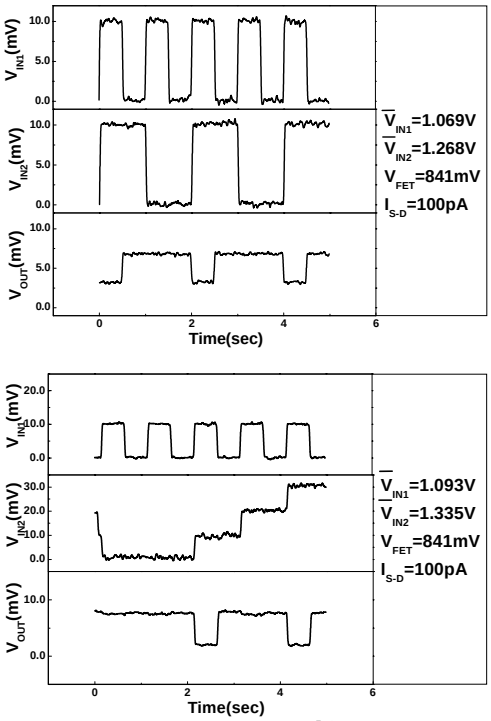
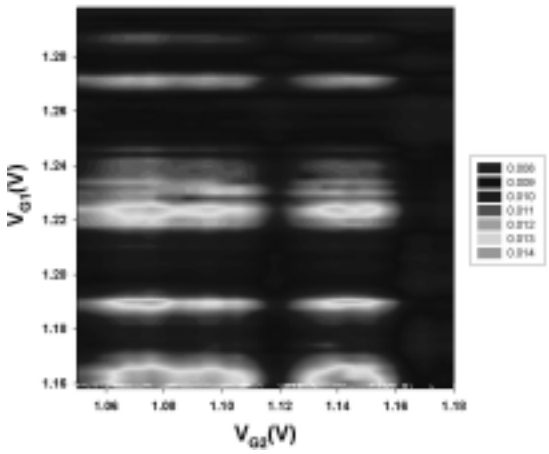


b)

Figure 2. (a) A grayscale contour plot of the voltage output Vout as a function of two SET input voltages of Vin1 and Vin2 for NAND gate. The CC load current is set to 100pA with a voltage limit of 20mV and the V_{FET} is set to 841mV. b) The input-output voltage transfer characteristics of the NAND gate. For two SET input voltages, i) SET1(binary) & SET2(binary), ii) SET1(binary) & SET2(4-levels), (c) SET1(3-levels) & SET2(5-levels).

to blockaded/tunneling current regimes; high for both SETs blockaded, while low for one or both SETs tunneled-through. The input-output voltage transfer characteristics measured at 4.2K are seen in Fig. 2b) & 3b), for NAND & NOR gates. Square waves are applied to the SETs as two input voltages V_{IN1} and V_{IN2}, which are binary, multi-valued and binary-MV mixed.



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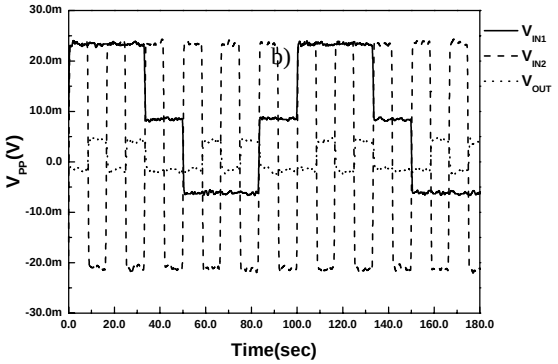

b)

Figure 3. (a) A grayscale contour plot of the voltage output Vout as a function of two SET input voltages of Vin1 and Vin2 for NOR gate. b) The input-output voltage transfer characteristics of the NOR gate: SET1(binary) & SET2(3-levels)

The offset values for V_{IN1} and V_{IN2} are selected in the periodic regime of the contour plot of V_{OUT}, as seen in Fig. 2a) & 3a).The resulting voltage output of V_{OUT} display typical NAND or NOR gate functions for various V_{OUT} binary or multi-valued two SET input voltages. This result implies that our SET/FET hybrid circuits provide highly flexible NAND functionality not only for binary inputs but also for MV input signals. Moreover, the switching functionality of our SET/FET logic gate can be enhanced to OR (AND) operation by utilizing a side gate incorporated to each SET for NAND (NOR) gates. After applying proper side gate voltage, the phase of Coulomb peaks of each SET can be shifted to be out-of-phase of that without applying side gate voltage, which results in transforming the SET current level from high to low. This phase control of Coulomb oscillations by side gate voltage is one of the unique characteristic of the SET-based logic cells and was already utilized to achieve the complementary SET inverter and SET/FET literal gates[2]. Finally, our experimental results were also successfully demonstrated by SPICE circuit simulation of the SET-MOSFET hybrid circuits including a half-adder, based on the parameter values of the SETs extracted from our experimental data.

This work was supported by MOST through the Frontier 21 National Program for Tera-level NanoDevices(TND) and, in part, by CKC Program for Nanoelectronics.

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[2] K.S. Park et al, IEEE Trans. Nanotechnol., Vol.4, No2, pp.242 (2005).