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Multi-Functionality of Novel Structured Tunneling Devices

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1. Introduction

As device dimensions approach nanoscale region, the physical limitations of MOSFETs become more evident. Also, with an emergence of increasing demand of mobile applications, much attention has been aroused in low-power and multi-functional devices. In order to overcome these issues, recently, some innovative devices have been proposed. Among them, tunneling devices shown in Fig. 1 are considered as one of the most promising ones. They have some advantages of good short channel behavior, low leakage current, small temperature dependence, and multi-functionality. This paper is mainly devoted to multi-functionality, which means using one transistor with four operation modes. As shown in Fig. 1, tunneling devices can be operated as n-/p-channel surface junction tunneling (SJT) devices [1] and tunneling field-effect transistors (TFETs) [2] depending on the bias conditions. Since the former uses the forward operation mode of p-i-n diodes, it features negative differential conductance (NDC) which makes novel circuit design possible [3]. On the other hand, the latter adopts reverse operation mode. It leads to normal transistor operation: saturated output current with the increase of drain voltage.

In this paper, we deal with SJT device and TFET operation characteristics of 70-nm novel structured tunneling devices. To the best of our knowledge, it is the first result to observe both device actions from one nanoscale transistor.

2. Device Fabrication

Fig. 2 illustrates the key process flow of a 70-nm tunneling device, most of which refers to that of Ref. [4]. An SOI wafer was selected as a substrate to suppress bulk leakage current. Firstly, n-type dopants were implanted into the SOI wafer (Fig. 2 (a)). Then, active region definition was followed by TEOS layer deposition (Fig. 2 (b)). The drain region was defined in a mesa shape (Fig. 2 (c)). After that, gate oxidation was followed by sequential poly-silicon and TEOS layer deposition (Fig. 2 (d)). Following sidewall-spacer gate formation, low-energy p-type ion implantation was performed to form the source extension region (Fig. 2 (e) and (f)). Subsequently, TEOS sidewall spacer was formed and then high-energy p-type ion implantation was done for source region formation (Fig. 2 (g)). Finally, wafers were annealed at 1000 ℃ for 5 seconds in an RTA tool (Fig. 2 (h)). In the proposed process, the gate, the source and the drain region are self-aligned. It makes nanoscale device fabrication cheaper and simpler. By applying the process steps shown above, 70-nm novel structured tunneling devices were successfully fabricated.

3. Electrical Characteristics

We used four biasing conditions to observe multi-functionality of the fabricated device as summarized in Table 1. By using Mode A, n-channel SJT device operation is observed. As shown in Fig. 4, it shows NDC when the gate voltage is 0.8 V. Its peak-to-valley current ratio (PVCR) is measured to be 1.2 at room temperature. Excess current due to the defects, which lowers PVCR, is suppressed by making the gate length larger around the edge of active layer as illustrated in Fig. 3. In the case of Mode C, the fabricated device successfully acts as an n-channel TFET. Since it uses reverse operation mode of p-i-n diode, we can not observe NDC but saturated output current as shown in Fig. 5. The reason of output current saturation has been already covered in Ref. [5]. When applying Mode B and D, no band-to-band tunneling effect is observed. It can be analyzed as follows. In the device structure shown in Fig. 2, the n-type drain junction is not as abrupt as the p-type source junction. It is because the drain junction is formed by high-energy implantation process. Thus, the tunneling probability between the channel and the drain at negative gate potential is much lower than that between the channel and the source at positive gate potential. If we make the drain junction more abrupt by using epitaxial growth, p-channel SJT device and TFET operation are expected to be observed.

4. Conclusions

A 70-nm novel-structured tunneling device was successfully fabricated and its multi-functionality was confirmed. They act both as an n-channel SJT device and an n-channel TFET depending on the bias conditions. P-channel device operation will be observed by making n-type drain junction more abrupt. In the case of the n-channel SJT device, it shows NDC with a PVCR of 1.2 at room temperature. On the other hand, output current is saturated with the increase of the drain potential in the n-channel TFET.

Acknowledgements

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References

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Table 1. Biasing conditions of tunneling devices

	Gate	N-type doped	P-type doped
Mode A	(+)	GND	(+)
Mode B	(-)	GND	(+)
Mode C	(+)	(+)	GND
Mode D	(-)	(+)	GND

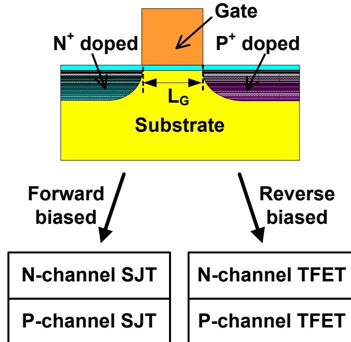


Fig. 1. Structure of the tunneling device. Depending on bias conditions, it can act as an n-/p-channel SJT device and TFET.

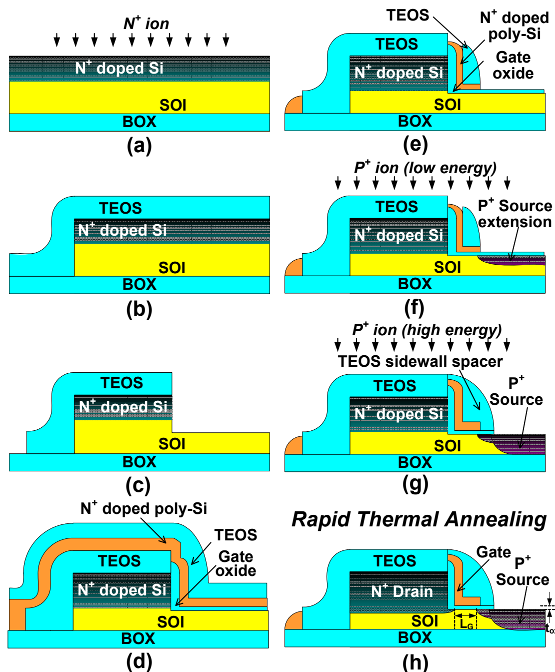


Fig. 2. Key process flow of the fabricated device.

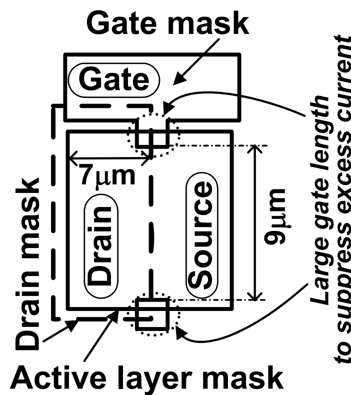
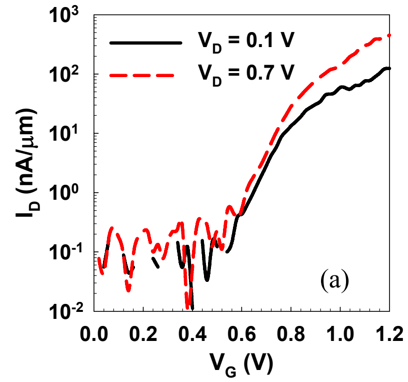


Fig. 3. Mask layout of the fabricated device.



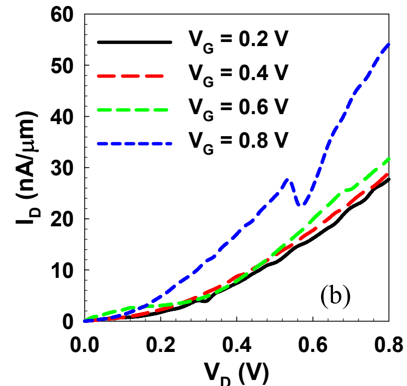
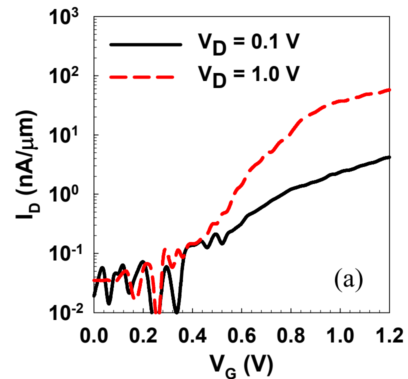


Fig. 4. (a) Transfer and (b) output curves of 70-nm n-channel SJT device (Mode A).



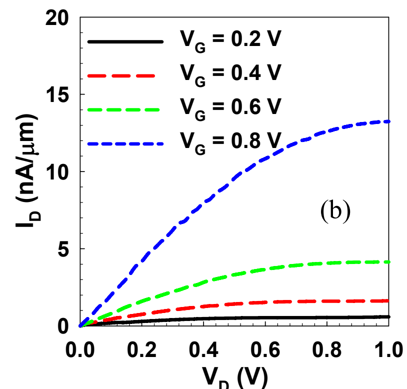


Fig. 5. (a) Transfer and (b) output curves of 70-nm n-channel TFET (Mode C).