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A Field-Effect Transistor with a Deposited Graphite Thin Film

Hiroshi Inokawa[1], Masao Nagase[2], Shigeru Hirono[3], Touichiro Goto[2], Hiroshi Yamaguchi[2], and Keiichi Torimitsu[2]

[1]Research Institute of Electronics, Shizuoka University, 3-5-1 Johoku, Hamamatsu 432-8011, Japan
Phone: +81-53-478-1308 E-mail: inokawa06@rie.shizuoka.ac.jp
[2]NTT Basic Research Laboratories, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi 243-0198, Japan
[3]NTT Afty Engineering Corporation, 2-35-2 Hyoue, Hachiouji 192-0918, Japan

1. Introduction

Recent observations have revealed that graphite, especially single- or few-layer graphite, is very attractive as an electronic material due to the extremely small effective masses and high mobilities of electron and hole [1]. However, the handling technique of few-layer graphite is still in its infancy, and there is not a clear prospect for extensive applications. Considering these, it is worthwhile to seek for the possibility of the deposited graphite thin films. Although such materials are usually polycrystalline and may not behave ideally, even a fraction of the intrinsic property is still valuable. Actually, M. Nagase, et al. recently reported the pseudo field-effect transistor (FET) using a carbon film deposited by electron cyclotron resonance (ECR) sputtering despite high parasitic series resistance of the probes and/or contacts [2]. Here, by using a thin-film FET structure with low parasitic resistance, the characteristics of the ECR-sputtered carbon film are investigated in detail.

2. Device Fabrication

FETs were fabricated using shadow mask depositions of carbon (50 nm) and metal (100-nm Au/10-nm Ti) from different incident angles. Figure 1(a) shows the plane view of the deposition mask, and the deposited metal/carbon films. The sizes of the suspended mask (L, W) were varied to obtain various channel lengths and widths of the FET. Figure 1(b) shows the cross-sectional view of the FET. The substrate is used as the gate, and the deposited metal is used as the source/drain electrodes (bottom-gate, top-contact structure). The gate oxide thickness is 20 nm.

The carbon films were deposited by ECR plasma sputtering at room temperature under the Ar pressure of 5×10^{-2} Pa. The deposition rate was 4.5 nm/min, and the ion acceleration voltage was approximately 20 V.

It is reported that this kind of film consists of 2~5-nm-scale crystallite of graphite [3]. The C 1*s* XPS spectrum shown in Fig. 2 can be decomposed into four peaks. The first two peaks at lower energies are assigned to sp^2 (C=C) and sp^3 (C-C) bonds, respectively, and their intensity ratio is 1:0.28, indicating that the film is rich in graphite. The sheet resistance of the 50-nm-thick film was measured by four-point probe to be 2.7 kΩ.

3. Electrical Characterization

Figure 3 shows the width dependence of the source-drain conductance. For positive W, the conductance is proportional to W as expected, and from the slope of the fitted line, and the sheet resistance by four-point probe, the parasitic series resistance is calculated to be 480 Ωμm. This is comparable to those of MOSFETs [4], indicating that the contact resistance is marginal. The temperature dependence of the conductance (inset) cannot be explained by simple thermally activated process. Hopping process might be a possibility [5], but more precise evaluation is needed.

Figure 4 is a logarithmic plot of the same conductance as in Fig. 3, showing the tail part of the conductance profile. The fitted curve is drawn on the assumption that the thickness distribution at the film edge is Gaussian with standard deviation of 65 nm (inset) and the conductance is proportional to the thickness. At the thin part of the thickness distribution, where the conductance is less than 10^{-8} S, modulation of the conductance by the gate electric field was observed by separate measurements with varied gate voltages.

Figure 5 shows the length dependence of the source-drain resistance. Since the channel area is shadowed from carbon deposition when L is larger than the height of the mask (0.5μm), the resistance increases rapidly. The devices with resistance higher than 10^9 Ω showed the field effect.

Figure 6 shows the drain current-gate voltage characteristics for L=0.75 μm and W=1.0 μm. The current increases on both positive and negative sides of the gate voltage (ambipolar characteristics), presumably reflecting the semimetallic nature of graphite. On-off current ratio tends to be larger for lower drain voltage and lower temperature. For V_D=0.5 V, the on-off ratios of two and seven were obtained at 294 and 150 K, respectively.

4. Conclusions

We investigated the field effect of graphite-rich carbon nanocrystallite thin films deposited by ECR-sputtering, using a bottom-gate top-contact FET structure. An appreciable ambipolar field effect was observed at the film edge where the thickness is vanishing. On-off current ratios of two and seven are attained at 294 and 150 K, respectively. The results are encouraging the further research on the deposited graphite thin films for electronics applications.

Acknowledgements

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References

[1] K. S. Novoselov, et al., *Science* 306 (2004) 666.
[2] M. Nagase, et al., *Jpn. J. Appl. Phys.* **45** (2006) 2009.
[3] S. Hirono, et al., *Appl. Phys. Lett.* **80** (2002) 425.

[4] K. K. Ng and W. T. Lynch, *IEEE Trans. Electron Devices* **ED-34** (1987) 503.
[5] K. Matsuda, et al., *Physica B* **329-333** (2003) 1529.

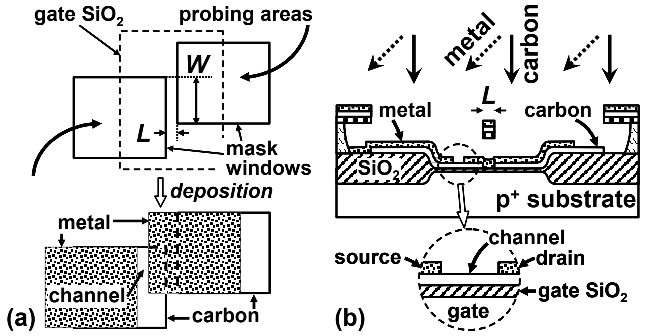

Fig. 1(a) Plane view of the deposition mask and deposited metal/carbon films, (b) cross-sectional view of the FET. Tow-step process of vertical deposition of carbon and oblique (45°) deposition of metal finishes the FET without additional lithographic process.

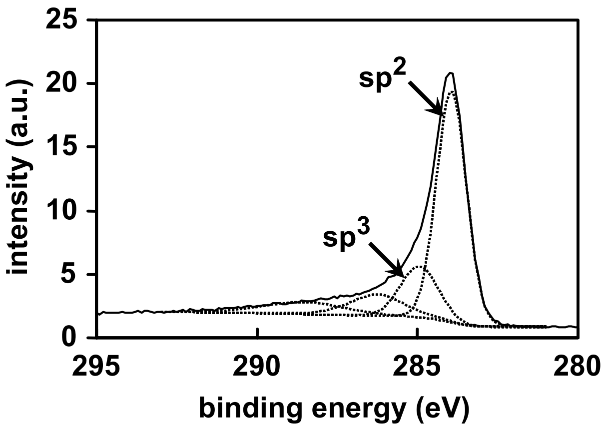

Fig. 2 C 1*s* XPS spectrum of the deposited carbon film. The sp^2 (graphite) component is dominant in the film. The small two peaks at higher energies are assigned to the C-O bond originated form the adsorbed oxygen [3].

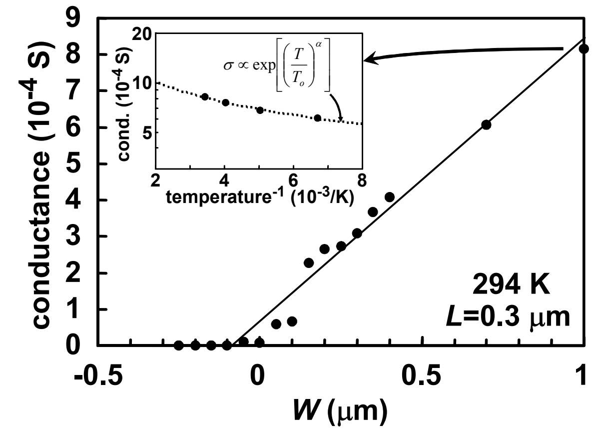

Fig. 3 Width dependence of the source-drain conductance of the devices with V_G=0. The slope of the fitted line is 7.8×10^{-4} S/μm. Inset: Temperature dependence of the conductance.

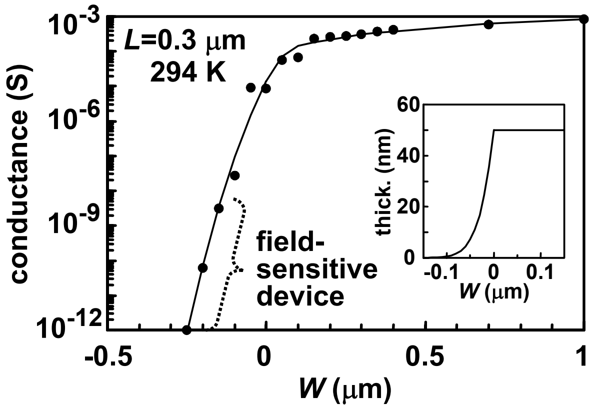

Fig. 4 Logarithmic plot of the same conductance as in Fig. 3, showing the feature of the tail part of the thickness distribution at the film edge. From the separate evaluation similar to Fig. 6, the devices with smaller conductance were found to be field-sensitive. Inset: Estimated thickness profile at the film edge.

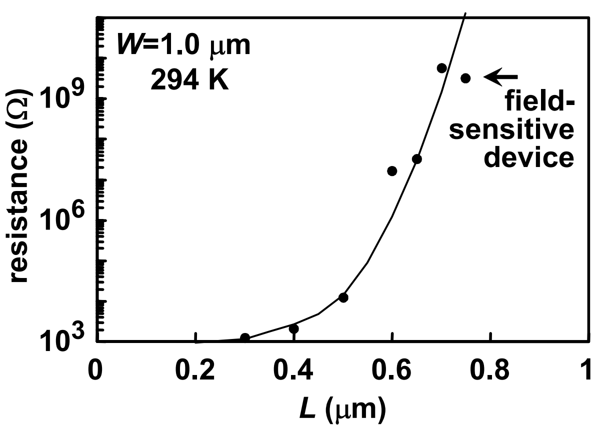

Fig. 5 Length dependence of the source-drain resistance of the devices with V_G=0. The resistance increases rapidly when the channel region is shadowed by the enlarged L (>0.5 μm). The devices with high resistance were found to be field-sensitive.

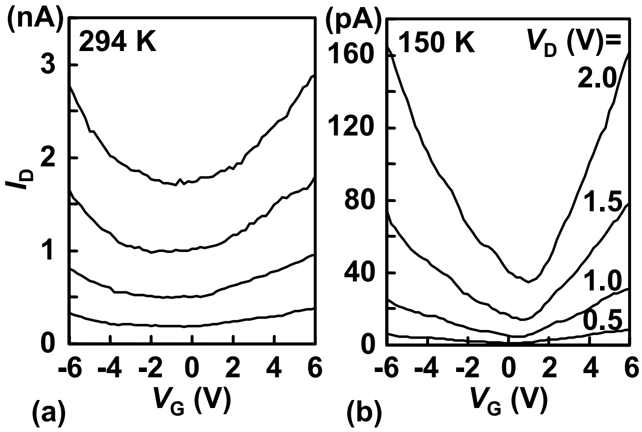

Fig. 6 Drain current-gate voltage characteristics for L=0.75 μm and W=1.0 μm at (a) 294 K and (b) 150 K, respectively. On-off current ratios of two and seven are attained, respectively.