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Room Temperature Demonstration of Variable Full Width at Half Maximum of Coulomb Oscillation in Silicon Single-Hole Transistor

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1. Introduction

A silicon single-charge transistor (SCT) is one of the most promising high functional devices that could be combined with future ultra-high density, ultra-low power CMOS VLSI circuits. The electrical control of the SCT characteristics, such as peak voltage V_{peak} of the Coulomb blockade (CB) oscillation or sharpness of the oscillation, is very important for adding further functionality to SCTs.

In this paper, full width at half maximum (FWHM) -the sharpness- of the CB oscillation in a single-hole transistor (SHT) has been successfully controlled at room temperature (RT) by means of the substrate capacitance (C_b) control using substrate depletion and accumulation/inversion (A/I) for the first time [1, 2]. The control of the peak sharpness was applied to the novel SCT analog pattern matching circuit [3] to achieve higher functionality.

2. Fabrication and Device Characteristics

C_b control is achieved by changing the substrate depletion layer by changing substrate bias V_{bs} [1, 2]. When the substrate is in A/I region, C_b is larger than that of depleted region. This is because the C_b in A/I region is determined by the BOX thickness (Fig. 1). Particularly, when the BOX is thin and the substrate impurity concentration is low, this modulation is significant.

Thus, we fabricated ultranarrow SHTs [4] with thin BOX whose initial thickness was 10 nm. The extremely narrow channels are fabricated by the same method in [4]. Before the gate oxidation, in order to remove the EB resist (HSQ), the samples are treated with HF, and the BOX under the ultranarrow wire is completely removed as shown in Fig. 1(a). The removed BOX is then refilled by the gate thermal oxidation and CVD oxidation (Fig. 1(b)) since the original BOX is thin enough to refill. The gate oxide thickness is 21 nm and the BOX thickness under the ultranarrow wire channel is estimated to be around 21 nm, because it is increased by the surface cleaning and the thermal oxidation. The formation of ultra-small dots and tunnel barriers for SHT operation in this process is described elsewhere [5].

Fig. 2(a) shows drain current I_d as a function of gate voltage V_{gs} at V_{bs} = 0 V in a fabricated SHT at RT. All measurements in this paper were performed at RT. Two large CB oscillations has been observed whose peak-to-valley current ratio (PVCR) are 31 and 11 at V_{bs} = 0 V, respectively. Fig. 2(b) shows clear peak shift of CB oscillation by applying V_{bs}. Fig. 3 shows V_{bs} dependence of the peak voltage shift ΔV_{peak} (= $V_{peak|Vbs}$-$V_{peak|Vbs=0V}$) for both peaks. The slope of Fig. 3 corresponds to γ (= $d\Delta V_{peak}/dV_{bs}$ = C_b/C_g, C_g is gate capacitance). We can clearly see a region where γ is nearly zero in both peaks. This is a strong evidence of the substrate depletion where C_b is small. The right/left region of the depleted area with large γ (large C_b) corresponds to the substrate A/I. No such clear modulation of the peak shift has been observed in SCTs.

Fig. 4 represents the relation between the peak shift and FWHM, the sharpness of the oscillation, of the first CB oscillation. Fig. 4 obviously shows the drop of the FWHM at the depletion region meaning that our device can change the FWHM electrically even after the device fabrication. As FWHM is inversely proportional to $\alpha = C_g/C_{dot}$ ($C_{dot} = C_g+C_s+C_d+C_b$) [6], where C_s, C_d and C_{dot} are source, drain and total dot capacitance respectively, the change in C_b results in modulation of FWHM. The second peak also shows similar behavior which is not shown here.

3. Application to the SCT Analog Pattern Matching Circuit

We demonstrate an application of the FWHM modulation of the CB oscillation to the SCT analog pattern matching circuit [3]. The key function in this circuit is the calculation of the distance (similarity) between the input and the stored data and it can be realized by just utilizing the shape of the CB oscillation, where V_{gs} corresponds to the input and V_{peak} to the stored data, which can be controlled by the nonvolatile memory operation using silicon nanocrystal floating dot [3]. When input V_{gs} is applied, the output I_d reflects the similarity between the stored data as shown in Fig. 5(a). The control of the peak sharpness here is taken as the strictness control of the similarity evaluation; therefore, the proposed SHT can realize this function by nature (Fig. 5(b)).

The modulation of the FWHM was roughly 10% according to Fig. 4, which is not enough for practical operation. However, it can be improved by optimizing the device design. The design method to increase the modulation is to change α (i.e. γ or C_b) drastically between the depletion and A/I region. Thus, substrate impurity concentration should be as small as possible for small C_b at substrate depletion, and maximize the coverage of the channel by substrate with thinnest BOX that is available for large C_b at substrate A/I. Also, C_s and C_d should be small enough so that the modulation of C_b can be fully transferred to the change in α. Ultranarrow wire channel process is known as the best fabrication method for this purpose [7]. Table. 1 shows the estimated modulation factor of the FWHM depending on α and γ at substrate A/I by simple calculation. Modulation factor rapidly increases at high α and γ. From the extracted α and γ from Fig. 4, 0.43 and 0.15 respectively, the calculated modulation factor 6.4 % slightly underestimates the measurement. More than 70 % of modulation would be possible if α and γ are made to 0.45 and 1.0 respectively.

4. Conclusions

Variable FWHM of the CB oscillation SHT has been demonstrated at RT by changing the substrate condition from depletion to A/I in thin-BOX SOI substrate. The control of the peak sharpness which is taken as the strictness of the similarity evaluation in SCT analog pattern matching circuit enables us to add further functionality to the application.

References

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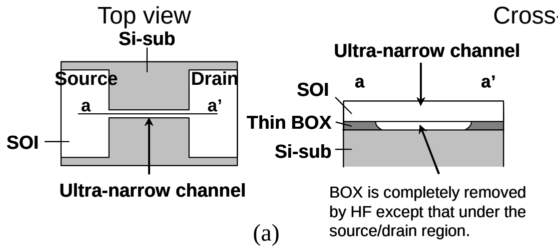

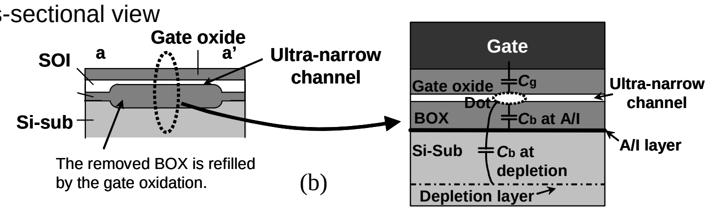

Fig. 1: Device structure of the fabricated SHT. (a): Before gate oxidation. Top view structure is also shown. (b): After gate oxidation. C_b is variable through substrate condition.

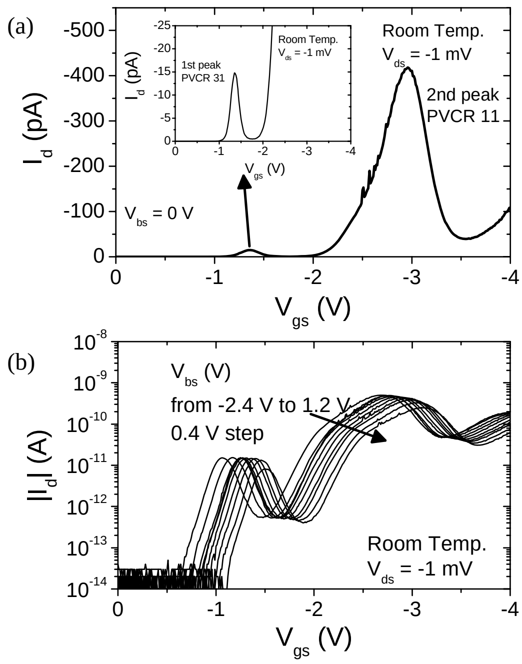

Fig. 2: (a): Measured I_d-V_{gs} characteristics of SHT at RT and V_{bs} = 0 V. Two CB oscillations with PVCR of 31 and 11, respectively are shown. (b): LogI_d-V_{gs} characteristics of same SHT with various V_{bs}. Clear I_d shift is observed.

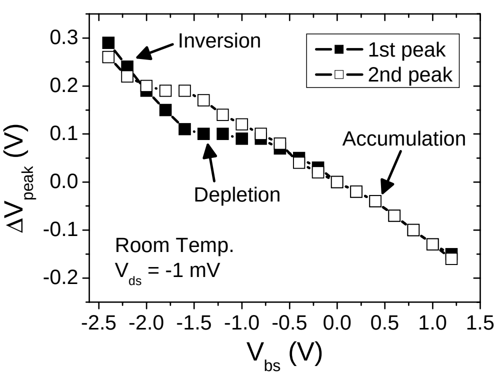

Fig. 3: V_{bs} dependence of ΔV_{peak} in Fig. 2(b). ΔV_{peak} is the difference between the V_{peak} at the present V_{bs} and that at V_{bs} = 0 V. Both peaks show clear substrate depletion region.

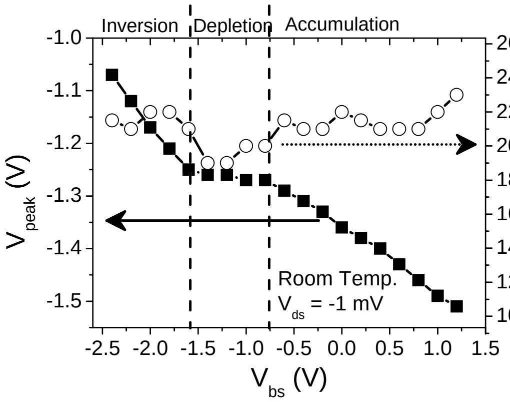

Fig. 4: Relation between V_{peak} and FWHM of the first CB oscillation. Value of the FWHM clearly decreases at the depletion region.

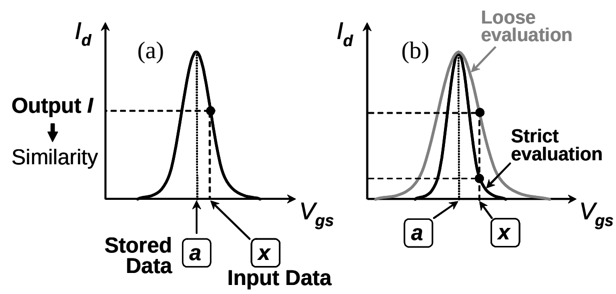

Fig. 5: (a): Schematic of analog pattern matching using SCT. If input V_g is near to the stored data V_{peak}, the output I_d is high showing the large similarity between the stored and input data. (b): Schematic of difference in FWHM (sharpness) in the application. Sharper oscillation performs stricter evaluation.

Table. 1: Calculated modulation factor of the FWHM as a function of α and γ at A/I region. C_b in substrate depletion was assumed to be 1/15 of that in A/I region considering the BOX thickness as 20 nm and substrate impurity concentration as 10^{15} cm^{-3}.

α \ γ	0.15	0.5	1.0	1.2
0.1	1.4 %	4.9 %	10.3 %	12.6 %
0.2	2.9 %	10.3 %	23.0 %	28.9 %
0.45	6.7 %	26.6 %	72.4 %	101.6 %
0.8	12.6 %	NA	NA	NA