Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 858-859

B-9-2

Deep Trench Isolation for Pixel Crosstalk Suppression in Active Pixel Sensor with 1.7µm pixel pitch

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1. Instruction

CMOS image sensor has been applied widely for mobile devices due to some significant advantages compared to charge coupled device image sensor. Recently, In order to accept higher pixel density within given or even smaller optical format, pixel dimension has been scaled down continuously. CMOS image sensors with sub-2µm pixel pitch have been reported. [1,2,3] As the pixel size decreases, degradation of pixel crosstalk, especially electrical component, is inevitable since it is getting harder to form the diffusion barrier to the thermal motion of optically generated electrons while maintaining the full well capacity or sensitivity characteristics. In this paper, we propose a novel pixel structure with deep trench isolation (DTI) to effectively suppress the crosstalk, while the full well capacity and sensitivity keep the same or even higher.

2. Device Design and Fabrication

Figure 1 illustrates the mechanism for crosstalk suppression by DTI which is about 3~4µm deep. As shown in Fig. 1(a), conventional STI structure does not fully prevent electrons from diffusing into adjacent pixels. The electron diffusion is generated around the quasi-neutral region in relatively deep photosensitive region, however isolated by electronic barrier made by relatively shallow ion implant. On the contrary, DTI structure, which is filled with materials with lower refractive index than silicon, could be effective to block electrical crosstalk in deep quasi-neutral region as well as optical crosstalk through active silicon (Fig. 1(b)). Moreover, the full well capacity and sensitivity could increase through minimization of p-type implant for photodiode isolation and increase of photodiode depth without hurting the crosstalk. We integrated the DTI into 1.7µm pixel array to suppress the crosstalk, which was fabricated using the 0.13µm CMOS technology. The details of the DTI process are as follows:

1) Firstly, STI is formed for peripheral and pixel transistors.
2) Secondly, deep trench is formed, and then in order to suppress white spot followed by uniform sidewall doping and trench oxidation.
3) Finally, the deep trench is filled with USG / HDP-Oxide and CMP is performed. The rest of process follows standard CMOS imager process.

Figure 2 shows the process flow and cross-sectional SEM image of pixel with DTI.

3. Experimental Results and Discussion

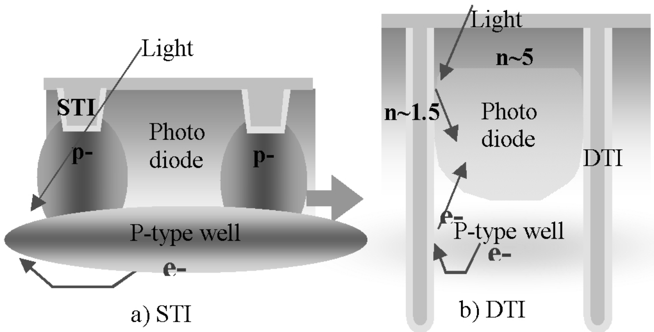
Figure 3 and 4 show the schematic diagrams of novel DTI-all-around and partial-DTI scheme. To fill the gap of DTI-all-around structure, some processes were modified, thus somewhat different from those of partial-DTI. Figure 5 shows the measured crosstalk, which is defined by the ratio of the sensitivity of optical black pixel to that of active pixel. STI is 0.4µm deep and DTI is partially formed to the depth of 4µm. The crosstalk of partial-DTI is lower than that of STI by 30%, and especially more significant at Red/Green pixels than Green/Blue pixels. This means the reduced crosstalk is mostly the electrical component. For further crosstalk suppression, DTI-all-around structure could be needed. To verify this, 3D simulations were performed in Fig. 6. It shows that about a half of photo- generated electrons is detouring around partial-DTI. Figure 7 shows the 2D crosstalk simulation result, which is believed to be similar situation to 3D DTI-all-around in terms of the electrical crosstalk. It is shown that the electrical crosstalk component could be largely suppressed by about 80% in the case of DTI-all-around as the trench depth increases. Figure 8, 9, and 10 show that the full well capacity, sensitivity and white spot could be controllable to keep or improve their characteristic levels through dopant profile optimization. Especially, white spot could be suppressed by shallow and uniform doping around DTI.

4. Conclusion

DTI process with 4µm deep trench has been developed and successfully applied to 5Mega CMOS image sensor with 1.7µm pixel pitch. DTI was found, from 2D/3D simulation and experiments, to be very effective to reduce electrical crosstalk without degrading other pixel characteristics such as the full well capacity, sensitivity, and white spot. Therefore, DTI technology could be a solution to offer better performance for CMOS image sensor with small pixel size of sub-2.0µm

5. Reference

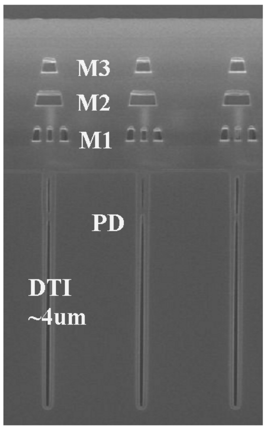
[1] C.R. Moon, et al., IEDM, p813, 2005.
[2] S. H. Lee, et al., VLSI, 2006, accepted
[3] H. Noh, et al., IEEE workshop on CCD and AIS., p197, 2005 .



a) STI b) DTI

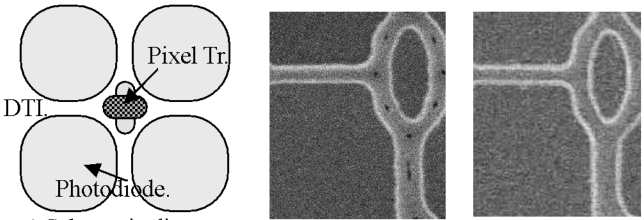
Figure 1. Illustration for crosstalk suppression mechanism of DTI structure.

1. Epitaxial growth on substrate
2. STI formation
   - for peripheral and pixel transistors
3. DTI formation
   - for photodiode
4. Well and channel implantation
5. Gate formation
6. Photo Diode formation
7. Source/Drain formation
8. Co-salicidation (PD blocked)
9. Metallization (3Met.for pixel)
10. Color filter and micro lens



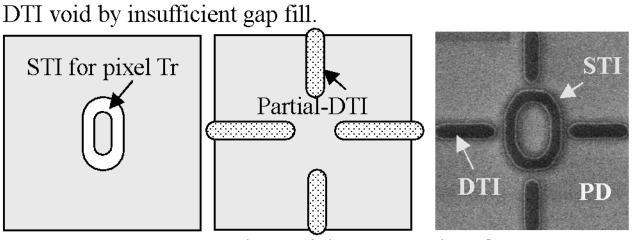
a) Process flow b) Cross-sectional SEM image

Figure 2. Process flow and cross-sectional SEM image



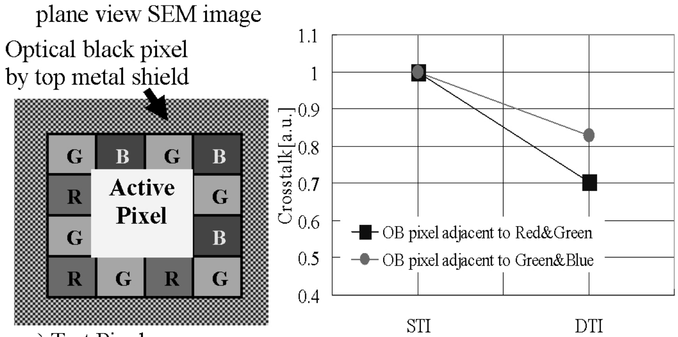
a) Schematic diagram b) DTI void c) DTI void free

Figure 3. Schematic diagram of DTI-all-around structure and DTI void by insufficient gap fill.



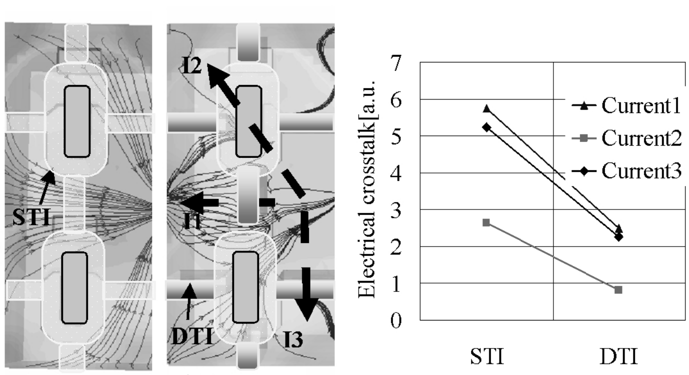
a) STI for pixel Tr. b) Partial-DTI b) After DTI CMP

Figure 4. Schematic diagram of partial-DTI structure and its final plane view SEM image



a) Test Pixel array b) Crosstalk

Figure 5. The measured crosstalk of optical black pixel



a) STI b) DTI c) Electrical crosstalk

Figure 6. Electrical crosstalk simulation for partial-DTI pixel

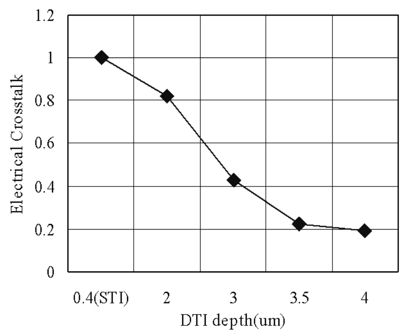


Figure 7. Electrical crosstalk simulation for DTI- all-around Pixel

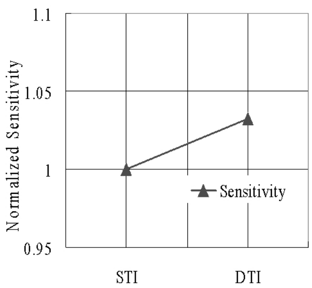


Figure 8. Measured sensitivity

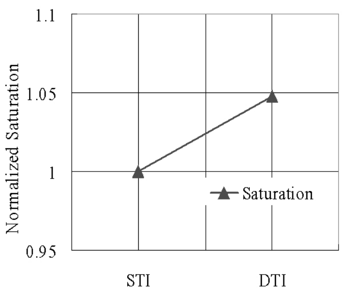
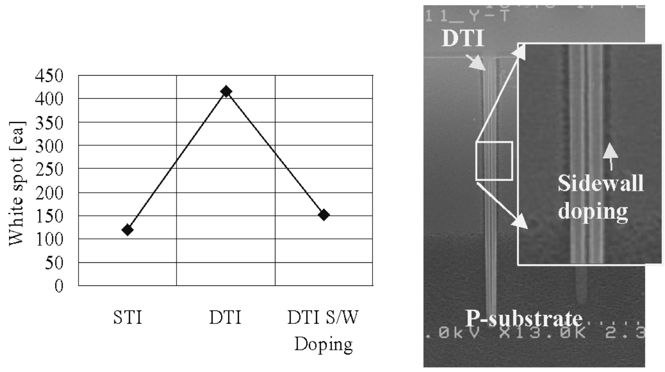


Figure 9. Measured saturation



a) Measured white spot b) Sidewall uniform doping

Figure 10. Improvement of white spot by uniform sidewall doping