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A Compact Single-Photon Avalanche Diode in a Deep-Submicron CMOS Technology

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1. Introduction

Single-photon detection using Geiger-mode single photon avalanche diodes (GM-SPADs) has become a powerful tool in a wide range of disciplines, from 3D imaging [1] to fluorescence spectroscopy [2]. Unlike other image sensors, such as CMOS Active Pixel Sensors (APS) or CCDs, which translate photon flux to collected charge, the information provided by a SPAD pixel is either digital, corresponding to the photon-arrival event, or analog, correlated to the precise time-of-arrival of the photon [3]. Upon its aggregation in time bins, this information can be used to generate a two-dimensional intensity distribution, similar to those gained with conventional sensors. The time-of-arrival information can be further used to study physical properties of single molecules [2] or to enhance fluorescent images by tagging pixels which exhibit characteristic photon-flux decays [4].

When operated in Geiger mode, SPADs are in essence reverse-biased pn junctions which can sustain numerous avalanche breakdowns, without incurring damage and with minimal charge trapping. When a photon is absorbed in the vicinity of the high-field region of the SPAD, it generates an electron-hole pair which may induce an avalanche through self-propagating impact ionizations. This avalanche can be electrically sensed with high timing accuracy, and is quickly quenched. The pixel is then reactivated by recharging the junction in excess of its breakdown voltage.

The physical requirements from a SPAD pixel are quite challenging. It must withstand electric fields in excess of 1 MV/cm (the breakdown field of silicon), instantaneous current densities above 0.3 μA/μm^2, and operate at voltages far higher than those of standard CMOS devices. As a result, SPADs have traditionally been manufactured using custom processes, and the required timing and processing circuitry has been bonded off-chip [2]. More recently, a CMOS SPAD has been manufactured on a 0.8 μm high-voltage commercial process. Due to the challenges mentioned above, a fill ratio of only 1% was achieved with a pixel area of 3,250 μm^2 – almost three orders of magnitude larger than CCD or APS pixels. Moreover, in order to achieve the sub-nanosecond timing accuracies required by most SPAD applications, more advanced technologies must be used.

We demonstrate a new single-photon avalanche diode device (Fig. 1), which utilizes the silicon-dioxide shallow-trench isolation (STI) structure common to all deep-submicron technologies, as the guard-ring. This makes it possible to achieve an order-of-magnitude improvement in fill factor and in pixel area, and results in improved SPAD performance. We present numerical simulations and preliminary experimental results from a test chip manufactured in an IBM 0.18 μm technology.

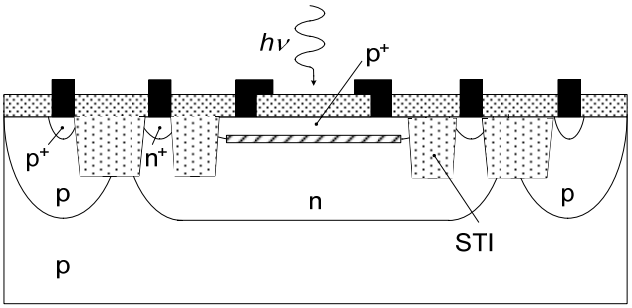

Fig. 1. STI-bounded SPAD: The silicon-dioxide trenches overlap the drain curved regions, thereby ensuring a uniform avalanche breakdown.

2. Modeling and Simulation

Physical Simulations

The devices were simulated using the ISE-DESSIS TCAD tool. The effect of a laterally-diffused curved junction can be seen in Fig. 2a. Premature breakdown at the high-field regions renders this device unfeasible as a Geiger-mode SPAD because the detection probability varies across the pixel. We also modeled the only other reported CMOS SPAD [1] (Fig. 2b). In this scheme, a triple-well structure is used to diffuse the p$^+$ drain implant at its edges

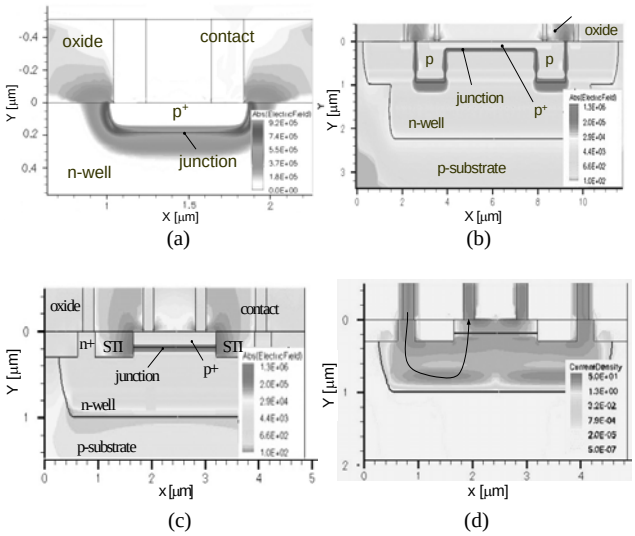

Fig. 2. Electrical field distributions in (a) a non-planar junction, illustrating localized breakdown; (b) Triple-well SPAD (c) New STI-bounded SPAD. (d) Current density plot of the new device.

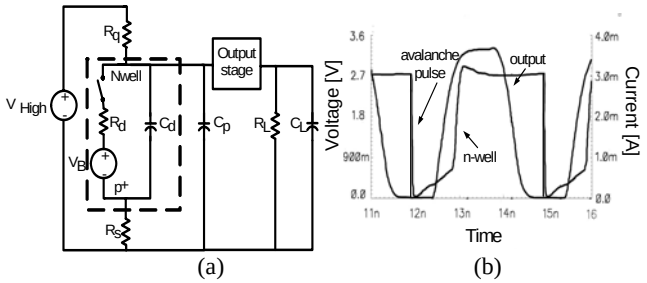

Figure 3. (a) Model of a passively-quenched SPAD pixel. On-chip structures are marked by a broken line. L, p and d subscripts stand for load, parasitics and diode. (b) Signal waveforms of actively-recharged pixel, corresponding to a 3 ns dead time.

to a surrounding p-well ring. The high-electrical field is concentrated mainly in the planar junction region, as desired. The new, more compact device is shown in Fig. 2c. The high electric field is confined between the trenches. The benefit of the STI structure as a guard-ring is illustrated in Fig. 2d. Charge carriers must circumvent the STI region, changing direction twice and thereby losing kinetic energy, before arriving at the anode.

Electrical Simulations

The SPAD device was modeled following the scheme developed by Cova [3]. A switch connected in series with the diode's resistance and in parallel with the junction capacitance models the device (Fig. 3a). In our device, the resistance is dominated by the space-charge resistance and is approximately 12.5 kΩ/μm^2 [5], while the depletion region's capacitance together with the input capacitance amounts to less than 50 fF. An avalanche breakdown is modeled as closing of the switch and a subsequent discharging of the capacitor. The avalanche is passively quenched by the quenching resistor, R_q.

Simulations show that the dead time, as constrained by the device recharge time, is 9 ns, compared with 32 ns in the fast SPAD reported by Rochas [6]. A new active recharge scheme has been implemented in order to further reduce this time while minimizing the effects of after-pulsing – the late release of trapped charges. In the new scheme, the recharge time is controlled externally, and the device remains either fully recharged or fully charged (Fig. 3b). The dead time is thus reduced to 3 ns, the lowest value to date, with benefits to many applications.

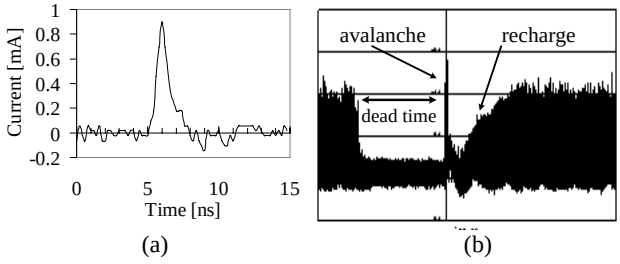

Fig. 4. Electrical characterization: (a) a single avalanche pulse equivalent to 1x10^6 electrons. (b) multi-scan image illustrating the SPAD dead and recharge times.

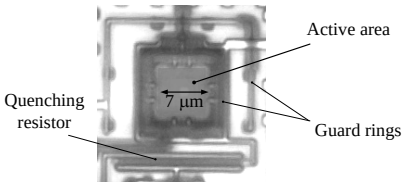

Fig. 4: Micrograph of an STI-bound SPAD pixel

2. Device Electrical Characterization

A test chip was manufactured in an IBM 0.18μm CMOS process through the MOSIS service. The chip was designed to prove the planarity of the new device and to prove its reliability to withstand numerous avalanches with the new guard ring.

The measured breakdown voltage of the STI-bounded device, 11V, matches the calculated voltage for a planar device of the same grading coefficient [8], proving that the junction is indeed planar.

Fig. 4 shows a micrograph of the new SPAD. Its fill factor is 9% for a 7 μm-diameter active area pixel, compared with 1% for the existing CMOS SPAD. Fig. 5a is an image of a single avalanche pulse corresponding to 1x10^6 electrons. Fig. 5b shows the dead and recharge times as measured on a Tektronix TDS3032 oscilloscope.

The first test device was quenched externally and as such exhibited a high dark current, similarly to other hybrid-quenched SPADs [9]. It operates continuously and with no shift in its DC characteristics over 5 x 10^{10} avalanche cycles. A second test chip is currently in production and is expected to provide jitter data and spectral response for this new device.

3. Conclusions

We introduced a new compact SPAD device, utilizing an STI guard ring, and demonstrated its reliable operation. An order-of-magnitude improvement has been demonstrated in fill factor and pixel size, opening the door for this device's integration into novel imaging systems.

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