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A Capacitive-Sensing Scheme for Control of Adaptive MEMS Device Stacked on CMOS LSI

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1. Introduction

Techniques for adaptively controlling the movable part of a MEMS structure, such as an RF-MEMS or optical MEMS switch, will allow us to enhance functionality of MEMS devices. The capacitive-sensing technique is a simple and effective way to detect a signal for the control of a movable MEMS structure [1,2]. Feedback control using capacitive sensing has been applied to the movable element stacked on a CMOS LSI (CMOS-MEMS) [3]. We focus on the MEMS variable capacitor stacked on an LSI as shown in Fig. 1. The capacitor is composed of a movable element, a control electrode, a sensor plate and a sensing circuit. When voltage is applied to the control electrode, the capacitance of the sensor plate C_s varies. Here, there is the problem in detecting C_s on the LSI: the parasitic capacitance C_p between the sensor plate and interconnects of the LSI is much larger than C_s. As a solution, we propose a capacitive-sensing scheme that detects a small sensed capacitance by effectively utilizing the parasitic capacitance. This paper describes the capacitive-sensing scheme for the control of the movable MEMS structure on the LSI. Next, the features of the proposed scheme are explained. Finally, the experimental results are presented.

2. Capacitive-Sensing Architecture

The architecture of the proposed sensing scheme features a shield plate structure and a ramp detection technique for enhanced sensitivity as shown in Fig. 2. The sensing circuit is composed of the shield plate, a current source, the ramp-detecting circuit, a reference-signal circuit, a phase detector and an integrator. The current controlled by the clock generates ramp signal due to parasitic capacitance C_p to the shield plate. The signal of the sensor plate generated by capacitance C_{sh} depends on the sensed capacitance C_s. The ramp-detecting circuit and the reference-signal circuit convert the ramp to the PWM signal. The phase detector outputs a pulse whose width changes according to the difference of the PWM signals. The integrator converts the summation of the pulse width in the sensing operation to the voltage.

The sensing circuit operation is explained in Fig. 3. When the clock changes from low to high, the voltage of the shield plate rises with the ramp due to C_p, while that of the sensor plate rises with the ramp depending on C_s. The voltage of the sensor plate is compared with V_{TH} and that of the shield plate is compared with V_{CTL}. The phase detector outputs pulse width Δt, which is approximated by

$$\Delta t \propto \frac{C_p}{C_{sh}} C_s . \qquad (1)$$

Equation (1) means that C_p, which is larger than C_{sh}, enhances the sensitivity for C_s. This is because charges to C_s become small due to increased charges to C_p. In this way, the sensed capacitance is detected utilizing the parasitic capacitance.

3. Experimental Results

The configuration of sensing circuit is shown in Fig. 4. The ramp-detecting circuit and the reference-signal circuit are composed of a comparator. The phase detector is an exclusive OR gate. The integrator uses a capacitance C_{itg} to sum the pulse width.

A test chip was fabricated with a 0.6-μm CMOS process and MEMS process [4]. The microphotograph of the test chip is shown in Fig. 5. The MEMS variable capacitor is stacked on the sensing circuit. The pads are used for C-V measurement. The characteristics of the chip are shown in Table I. The supply voltage of the sensing circuit is 3.3V and the tuning voltage of the MEMS variable capacitor is below 6.0 V. The characteristics of the sensing circuit are shown in Fig. 6. The sensed capacitances were measured with a C-V meter. The output voltage is proportional to the sensed capacitance. The sensing circuit has the sensitivity of 500 mV/fF, and the sensing time is 1 μs. These results confirm that the proposed sensing scheme is effective for the control of MEMS structures stacked on an LSI.

4. Summary

We proposed a capacitive-sensing scheme that utilizes the parasitic capacitance to enhance the sensitivity. The scheme features a shield plate structure and a ramp detection technique. The developed sensing circuit has the sensitivity of 500mV/fF. The proposed scheme will pave the way for adaptive MEMS devices on CMOS-MEMS.

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References

[1] B. Amini, et al., *ISSCC Dig. Tech. Papers* (2006), 288.
[2] Trey Roessig, et al., *Proc. of ECOC* (2002) 2.26.
[3] J. Terada, et al., *SSDM Ext. Abst.* (2005) 926.
[4] K. Kuwabara, et al., *SSDM Ext. Abst.* (2005) 86.

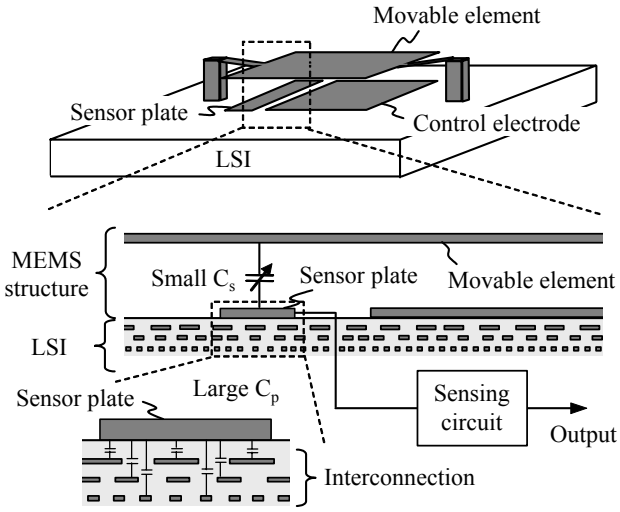

Fig. 1. MEMS variable capacitor stacked on LSI using capacitive-sensing to control the movable element.

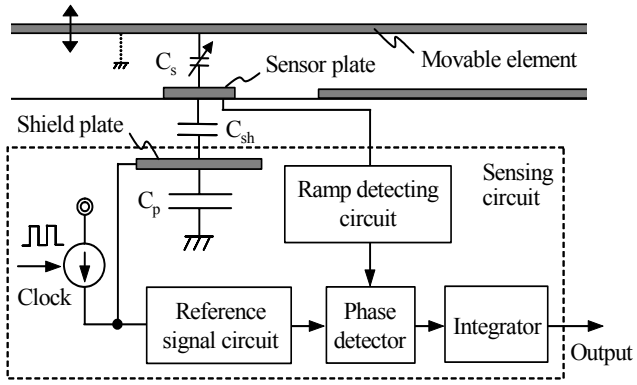

Fig. 2. Architecture for the proposed capacitive-sensing scheme.

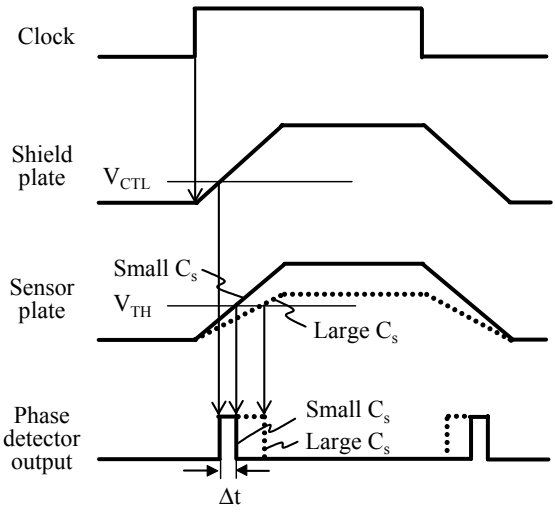

Fig. 3. Sensing circuit operation.

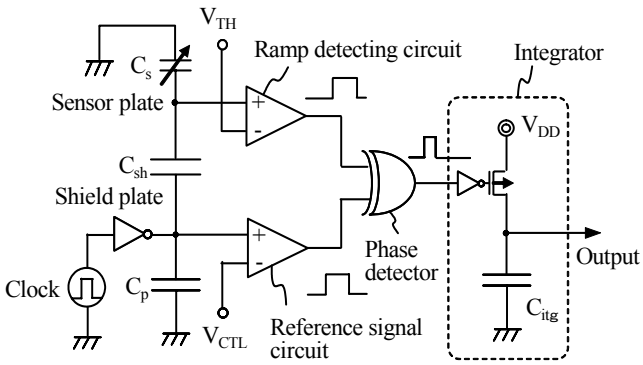

Fig. 4. Configuration of sensing circuit.

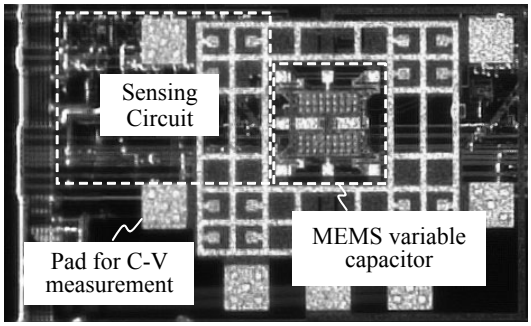

Fig. 5. Microphotograph of the test chip with the MEMS variable capacitor.

Table I Characteristics

Process		0.6-μm CMOS + MEMS process [4]
Sensing Circuit		
	Supply Voltage	3.3 V
	Clock Frequency	20 MHz
	Sensitivity	500 mV/fF
	Sensing Time	1 μs
	Power	4.5 mW
	Area	416 μm x 344 μm
MEMS Variable Capacitor		
	Tuning Voltage	< 6.0 V
	Area	200 μm x 200 μm

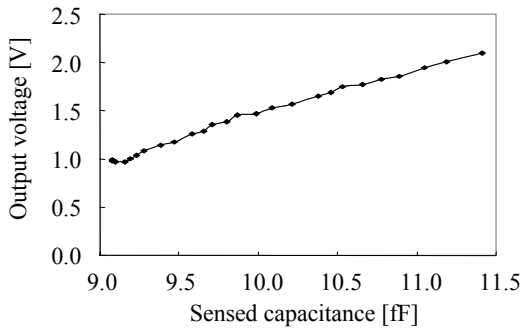

Fig. 6. Sensed capacitance vs. sensing circuit output (measured).