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On-Chip Asymmetric Coaxial Waveguide Structure for Chip Area Reduction

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1. Introduction

The development of high frequency circuits using CMOS process technology has been progressing rapidly in recent years [1]. With the scaling of CMOS processes to sub-100nm, transistors can perform better with higher cut-off frequency beyond 100-GHz. The performance of the passive devices, however, needs to be improved to exploit the performance of the transistors. In particular, the transmission line should be improved as it is the most basic structure for realizing other devices such as baluns and impedance transformers. It is noted that the area occupied by passive devices should be minimized to save chip area [2]. In addition, advanced CMOS processes require design for manufacturability (DFM) [3] that includes antenna rules which limit the performance of the transmission lines. In this work, a new asymmetric coaxial waveguide (ACW) transmission line structure is designed and fabricated to satisfy the above requirements.

2. New ACW Structure

This new structure shown in Fig. 1 is designed with the pad metal as part of the ground structure which encloses a signal conductor. The signal conductor of our test structure is designed with a width of 12μm surrounded by ground metals on the sides as well as its top and bottom. The side ground metals are at w_g=44μm from the signal conductor. The top pad metal is designed with slot patterns and grounded. This thick top pad metal layer is not suitable to be used as the signal line due to DFM reasons. The bottom metal is a slotted ground shield that prevents the electric field from penetrating the conductive silicon substrate. All the ground metals are connected together using inter-metal vias. Designed for our six-metal 90nm CMOS process, dummy ground metal is inserted between the signal line and the coplanar ground metal. No return current flows in these dummy ground metal because they are not connected together in the direction of the signal flow.

The capacitance is determined by the distance between the signal and ground potential which increases with reducing distance. The inductance is determined by the distance between the signal path and the return current path which increases with increasing distance. Therefore, a trade-off exists between increasing the inductance and capacitance of the coplanar waveguides (CPW) and the microstrip line to decrease the phase velocity, v_p given in (1) to achieve short wavelengths.

$$v_P = \frac{1}{\sqrt{LC}} \tag{1}$$

Equation (1) is considered for a lossless case to demonstrate the relation between the phase velocity and the line reactances. However, through innovative designs, the return current does not necessarily have to flow in the closest metal of ground potential. The ACW achieves this by keeping the capacitance large with closely-located slot metals at the top and bottom where the return current cannot effectively flow. Instead, the return current is forced to flow at a farther distance at the sides. This results in a large inductance, as illustrated in Fig. 2. The wavelength of the signal wave is related to the phase constant:

$$\lambda = \frac{2\pi}{\beta} \tag{2}$$

where λ is the wavelength and β is the phase constant. Hence, a large β results in a small λ and this corresponds to a shorter physical length to achieve a given fraction of the wavelength. Therefore, devices such as filters that require a determined wavelength can be fabricated using this structure to occupy a smaller the area on the chip.

3. Measured Results

The ACW is measured up to 110-GHz with Anritsu ME7808 with transmission reflection modules. The micrograph of the ACW is shown in Fig. 3. Fig. 4 shows a high phase constant that results in a short wavelength related by (2). Compared with the CPW and the microstrip line, it has a 3.3-times higher value. In addition, the ACW has a higher quality factor (Q-factor) as shown in Fig. 5. All the lines are fabricated using the same process with a width of 12μm and impedances between 20 and 50 ohms. As a result, circuits such as oscillators can achieve a significant area reduction as illustrated in Fig. 7.

4. Conclusion

A new ACW structure is presented for advanced CMOS processes which consists of a signal line surrounded by ground metals. This design increases the Q-factor and reduces the phase velocity for short wavelengths through large capacitance and inductance. The high measured value of the phase constant confirms the short wavelength of the signal propagating in this structure. Up to 110-GHz, the physical length of the new ACW is reduced down to 30% while achieving the same wavelength as conventional lines.

Acknowledgements

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References

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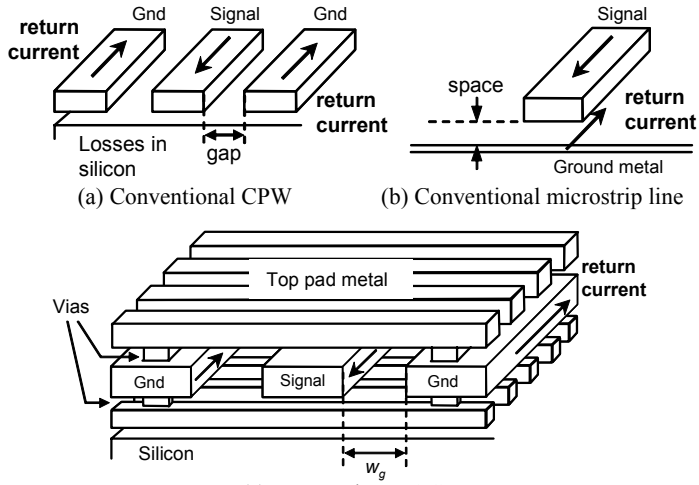


(a) Conventional CPW (b) Conventional microstrip line

(c) Proposed new ACW

Fig. 1 All structures are fabricated on a 90nm six-metal process. The capacitance of the ACW is determined by the distance between the signal and the top and bottom metals due to their proximity. The inductance is determined by the distance between the signal and the side ground metal where the return current flows.

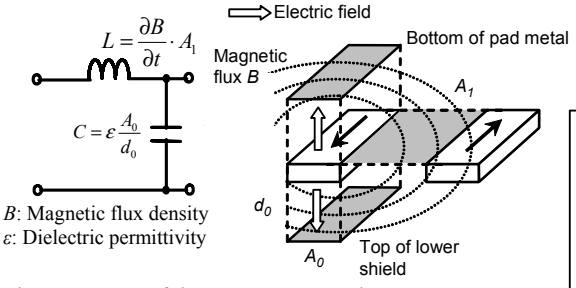


Fig. 2 Concept of the ACW. Increased area A_1 enclosed with farther side ground metals results in a larger inductance. d_0 is the decreased distance between the signal line and ground potential which allows larger capacitance to be achieved

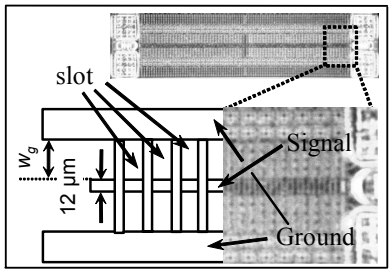


Fig. 3 Micrograph of the ACW.

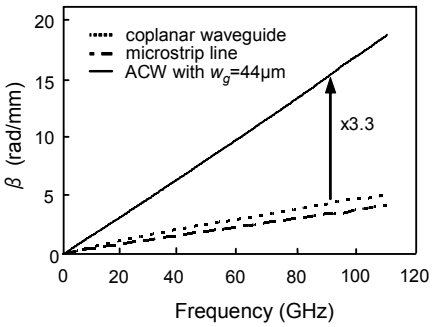


Fig. 4 Measured phase constant of the transmission lines. Large β results in a small λ to achieve a shorter physical length.

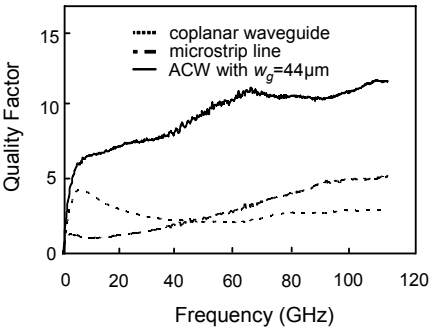


Fig. 5 Measured quality factors of the transmission lines where the ACW has the highest quality factor.

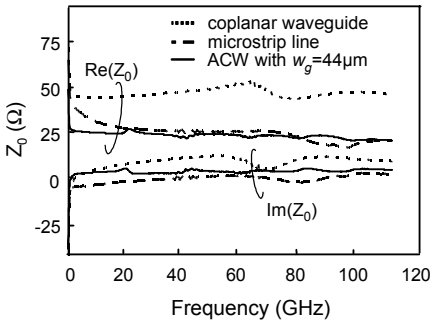
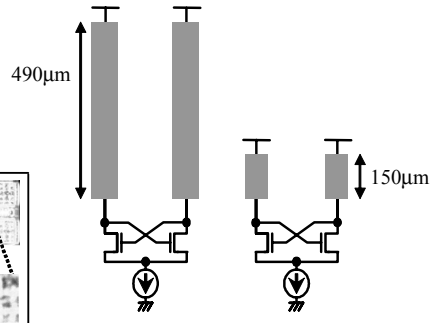


Fig. 6 Measured characteristic impedance of the lines. The lines have impedance between 20Ω and 50Ω.



(a) CPW (b) ACW

Fig. 7 Comparison of 60-GHz oscillators with quarter-wavelength transmission lines.