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On-Die Monitoring of Substrate Coupling for Mixed-Signal Circuit Isolation

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1. Introduction

Systems on a chip design always needs good isolation of analog circuits from digital circuits, in terms of suppressing substrate crosstalk. Decoupling measures often used in a CMOS technology include vertical isolation by deep n-well or SOI and lateral insertion of p+, n+, n-well or deep n-well guard rings. Here, the strengths of isolation vary not only with their structures and physical dimensions such as widths or areas but also with parasitic impedances on the paths to the system ground in a practically assembled chip, and highly depend on crosstalk frequencies as well. Although those structures can be precisely characterized by way of wafer-level S21 measurements on dedicated high frequency test patterns, and modeled in a form of equivalent circuits for estimation of isolation in a design stage [1], it is often unclear how much isolation has been effectively achieved in a realistic chip environment.

An on-chip waveform acquisition using source follower and latch comparator circuits was performed to evaluate substrate noise from CMOS digital circuits and showed clear dependency on package parasitics [2]. Frequency-dependent substrate coupling was characterized in a frequency domain especially for radio frequency circuits, using a frequency conversion function of a mixer circuit [3]. These measurement techniques successfully addressed the complexity of substrate coupling as mentioned, however, their use has been limited to the experimental test chips. On the other hand, the demand of short turn-around-time in SoC developments needs a simple and low cost way to check the proper use of isolation techniques in a current design, which will be fed back to a future design.

This paper proposes an on-die monitoring technique of substrate coupling applicable to a general mixed-signal chip, which reports actual isolation effectiveness in a packaged die and provides useful link with the modeling and simulation technology for isolation design.

2. System definition and simulation

Figure 1 describes an overview of an experimental chip applied with the on-die substrate coupling monitor. We assume that a chip is processed in a p-type bulk CMOS technology and mounted in a package as well as on a PCB board. Since numerous p+ substrate contacts in I/O rings at chip periphery as well as those distributed within circuits connects to the system ground (GND) through impedance paths, substrate coupling is frequency dependent and inherent to the actual chip environment.

When an radio frequency (RF) signal with the frequency of F_{RF} is introduced at one of injection points on the chip, substrate current diffuses within the chip, flows out to GND, and determines potential distribution. The RF voltage seen at the node of detection is input to the RF port of a mixer, which is also applied with a local (LO) signal with the frequency of F_{LO} from an external source at the LO port. The output from the mixer is evaluated off-chip at the very low frequency of $F_{OUT} = |F_{RF} - F_{LO}|$. It is noticed that the introduction of RF and LO signals into the chip is much easier than leading attenuated high frequency signals out from the chip, since the former can be large-signal and even rectangular shaped rather than sinusoidal. The magnitude of the signal at F_{OUT} relates linearly with the strength of substrate coupling between the points of injection and detection, as long as the signal level is smaller than the compression point of the mixer. We have simulated the on-die monitoring of substrate coupling, according to the design flow of Figure 2. The design of a mixer-based detector circuit is initiated with a harmonic-balance simulator (ADS) and finalized with a circuit simulator (SPICE). The silicon substrate was modeled as a resistive mesh (Figure 1), which is proved to be valid for the frequency less than 10 GHz. We have applied F-matrix computation flow [4] to derive a substrate model including the resistive mesh, guard-ring structures with p+, n+, or n-well, and explicit ports to connect to the impedance paths to GND as well as to the RF source and the mixer. The entire schematic of Figure 1 was represented in a single equivalent circuit netlist and simulated in Spectre RF with PSS functionality.

Figure 3 shows simulation results. As for the substrate coupling given in Figure 3(a), the RF signal seen at the point of detection is attenuated from the signal level of injection, depending on the distance from the point of injection. It is also shown that the use of p+ guard ring provides higher isolation against substrate coupling. The attenuated 1-GHz signal at the point of detection is input to the mixer along with the LO signal at 1.05 GHz, and the frequency components of the output is derived as in Figure 3(b). The signal strength at F_{OUT} of 50 MHz measures the effect of guard ring, and we can reproduce the signal level at the detection point from the measured signal strength by multiplying the conversion gain of the mixer.

3. Detector prototype and measurements

Figure 4 proposes the detector circuit for the on-die substrate coupling measurement. We have added a p-channel source follower (pSF) at the input of a double balanced mixer (DBM), for the purpose of DC level shift from the nominal substrate voltage at 0.0 V. In addition, an n-channel source follower (nSF) at the output drives F_{OUT} signal toward off-chip measurement equipment. A prototype of the detector fabricated in a 0.35-μm CMOS technology was tested. Figure 5 shows measured characteristics among the signal strengths of input at F_{RF} = 75 MHz and output at F_{OUT} = 5 MHz, in comparison with simulation. The measurements on the detector with nSF at the output achieves better agreement with the simulation, showing that nSF suppresses the loading disturbance imposed by the off-chip equipments. Also, the detector provides wide input range of 40dB for linear conversion, allowing us to evaluate a variety of isolation structures against substrate coupling. Although the measurement frequency is limited due to our experimental setup, the results are fit with typical clock frequency of low power digital circuits on a mixed-signal chip.

Figure 6 demonstrates the on-die substrate coupling evaluation. The RF signal at 135 MHz with various amplitudes is introduced to the center of the chip, and the

output from the detector provided with a rectangular LO signal at 140 MHz shows the strength of the substrate coupling. The waveform measured at the detector output and calculated FFT spectrum are also shown.

4. Conclusion

We have proposed on-die monitoring technique to evaluate substrate coupling in a practically packaged chip. A mixer-based detector circuit fabricated in a 0.35-μm CMOS technology successfully demonstrated the technique.

Acknowledgments

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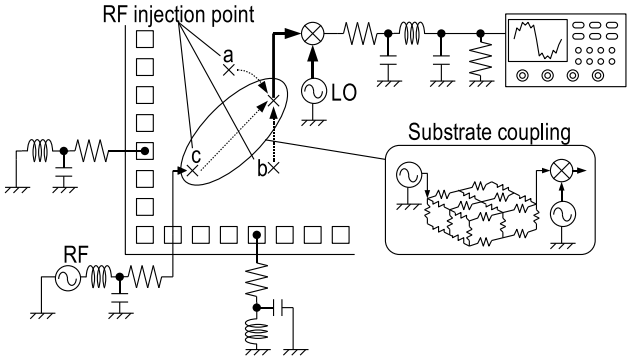

Fig. 1: Overview of on-die substrate coupling measurements.

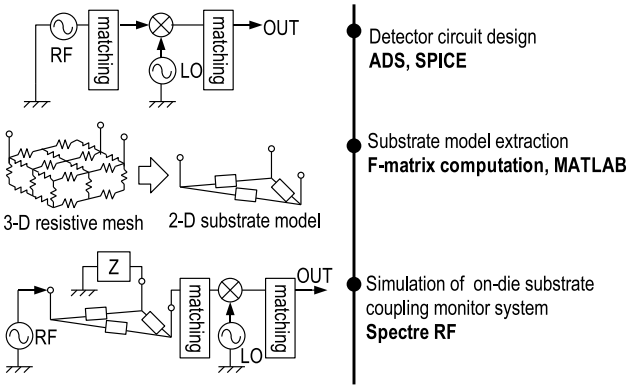

Fig. 2: Design and analysis flow of on-die substrate-coupling monitor system.

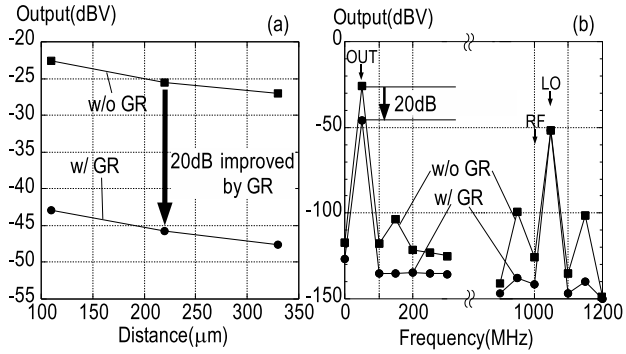

Fig. 3: Simulation results. (a) Substrate coupling, and (b) Detector output frequency spectrum.

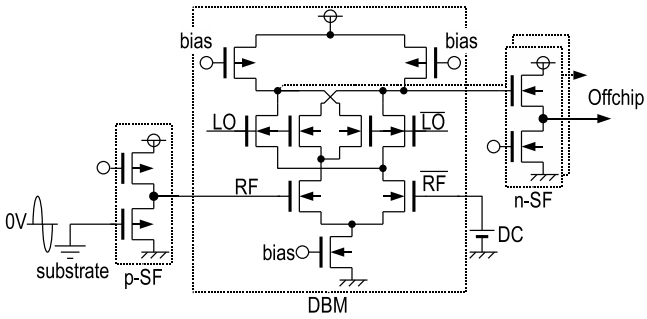

Fig. 4: Detector circuit diagram.

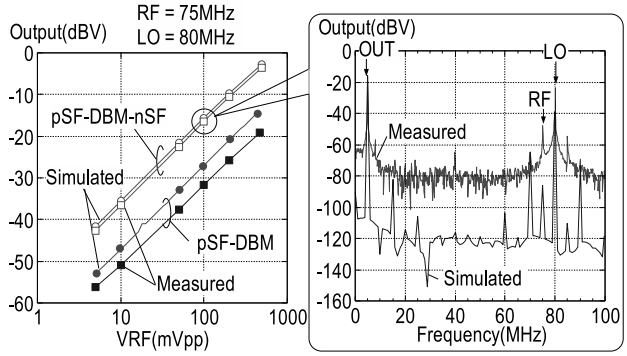

Fig. 5: Relation of signal strengths at input and output. Measurements and simulation are compared.

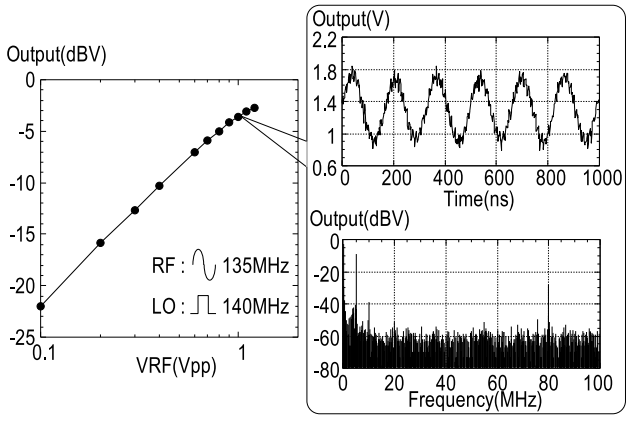

Fig. 6: On-die substrate coupling evaluation examples.