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60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique

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1. Introduction

The demand for 3D-stacked System in a Package (SiP) is increasing rapidly. A 3W 1Tb/s CMOS Inductive-Coupling data and clock link was developed by arranging 1024 data transceivers with a pitch of 30μm [1]. To reduce power dissipation, transmitter circuits (Tx) have been improved [2]. However, there is no report on improvement of receiver circuits (Rx).

This paper reports current-sensing technique in a receiver which can reduce 60% power dissipation compared with conventional voltage-sensing technique.

2. Testchip Design and Experimental Setup

Figure 1 shows the schematic of conventional voltage-sense receiver and proposed receiver using current-sensing technique. Current-sense receiver detects the current flowing in Rx inductor, I_{2C} directly. In voltage-sense receiver, the voltage across $R_{in,}$ is converted to current by the differential pair. In the case of the limited transceiver size, the current-sense technique is advantageous than the voltage-sense technique since the differential pair is not required.

A test chip is designed and fabricated in a 0.18μm CMOS. Chip microphotograph is depicted in Figure 2. The transmitters and receivers are arranged with a pitch of 20μm.

Figure 3. shows the experimental setup. Two testchips are mounted on two boards that are placed face to face in distance of 5μm. Communication distance is adjusted by a micromanipulator with accuracy of 1μm. Using alignment marks and infrared light enables adjustment of chip alignment.

3. Experimental Results

Measured BER dependence on total power dissipation is shown in Figure 4. By current-sensing technique, total power dissipation is reduced by 3.4mW/ch (60%) compared with conventional voltage-sensing technique without degrading both data rate(1Gb/s) and BER($<10^{-12}$).

Figure 5 shows the measured and simulated total power dissipation dependence on bias voltage (V_{bias}). In both receivers, $M_{V1,V2}$ and $M_{C1,C2}$ should operate in saturation region to obtain enough gain. In voltage-sense receiver, small size of $M_{V1,V2}$ (4μm/0.36μm) are used for high frequency operation. On the other hand, relatively large size is chosen for $M_{C1,C2}$ because they do not affect the operation speed. The simulated curve (dotted line) indicates that very large size (W/L= 24μm/0.36μm) is required for $M_{V1,V2}$ to reduce the power dissipation in the voltage-sense receiver to the same power of the current-sense receiver.

4. Discussion

Comparison of current-sense receiver with voltage-sense receiver from the viewpoint of circuit topology is depicted in Figure 6.

I_{2C} and I_{2V} are described as below in simplified model of inductive-coupling channel (Figure 6(a),(b)).

$$I_{2C} = \frac{\omega k\sqrt{L_1L_2}V_1}{\sqrt{\left\{R_1R_2-(1-k^2)\omega^2L_1L_2\right\}^2+\omega^2(L_1R_2+R_1L_2)^2}} \cong \frac{\omega k\sqrt{L_1L_2}V_1}{R_1R_2} = \frac{\omega k\sqrt{L_1L_2}V_1}{R_1(R_{L2}+2R_{inC})} \propto \frac{1}{R_{L2}+2R_{inC}}$$

$$I_{2V} = g_m V_{2V} = g_m I'_{2V} 2R_{inV} \cong g_m \frac{\omega k\sqrt{L_1L_2}V_1}{R_1R_2} 2R_{inV} \propto g_m \frac{2R_{inV}}{R_{L2}+2R_{inV}}$$

Note that R_1 is output resistance of Tx. R_2 is input resistance of Rx. L_1,L_2 is self inductance of Tx, Rx inductor. R_{inC} is input impedance of current-sense receiver. R_{L2} is parasitic resistance of Rx inductor. k is coupling coefficient. g_m is transconductance of $M_{V1,2}$.

In Figure 6, the dotted line indicates that very large size (W/L= 24μm/0.36μm) is required for $M_{V1,V2}$ to reduce the power dissipation in the voltage-sense receiver to the same power of the current-sense receiver.

In addition to the low power operation, proposed current-sense technique has large immunity to the device mismatch. Figure 7. shows the required transmit power as a function of the mismatch of differential pair ($M_{V1,V2}$ or $M_{C1,C2}$). 6σ of the V_{th} mismatch is assumed to be 25mV in this case. The V_{th} mismatch generates DC offset current. The DC offset current in the voltage-sense receiver flows into the cross-coupled transistors whereas the offset current flows into the Rx inductor in the current-sense receiver. As a result, the V_{th} mismatch is much relaxed in the current-sensing receiver and the required transmit power dose not affected by the V_{th} mismatch.

5. Conclusions

In this work, current-sensing technique is proposed and investigated. Current-sensing technique saves total power dissipation by 60% without sacrificing data rate(1Gb/s) and BER(<10^{-12}).

Acknowledgement

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References

[1] N. Miura, et al., "A 1Tb/s 3W Inductive-Coupling Transceiver for Inter-Chip Clock and Data Link," ISSCC Digest of Technical. Papers, pp. 424-425, Feb. 2006.

[2] M. Inoue, et al., "Daisy Chain for Power Reduction in Inductive-Coupling CMOS Data Link," to be published in Symp on VLSI Circuits, Jun. 2006.

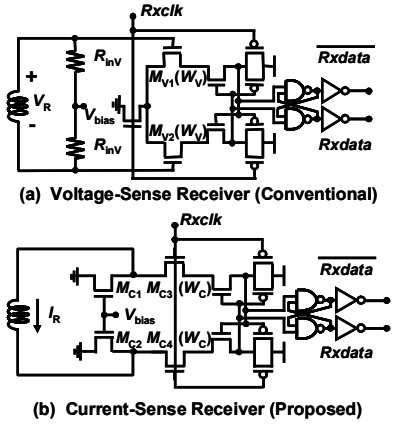

Fig.1 Schematic of voltage-sense receiver (conventional) and current-sense receiver (proposed).

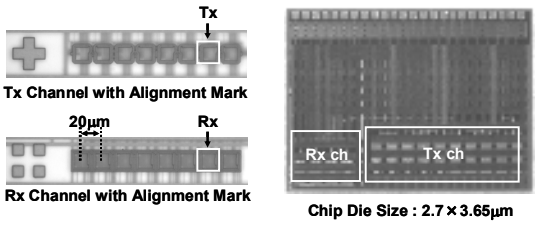

Fig.2 Chip microphotograph.

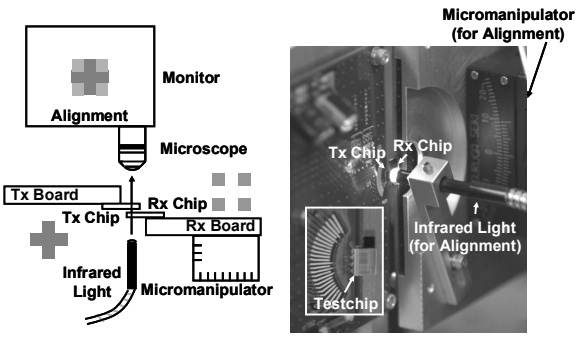

Fig.3 Experimental setup.

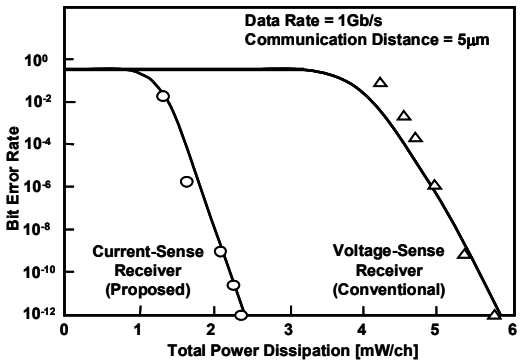

Fig.4 Measured BER dependence on total power dissipation.

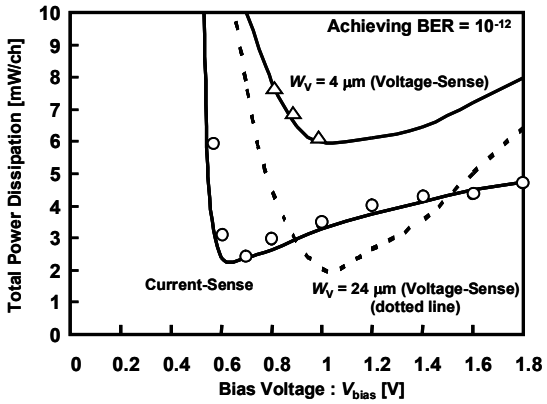

Fig.5 Measured and simulated power dissipation dependence on bias voltage.

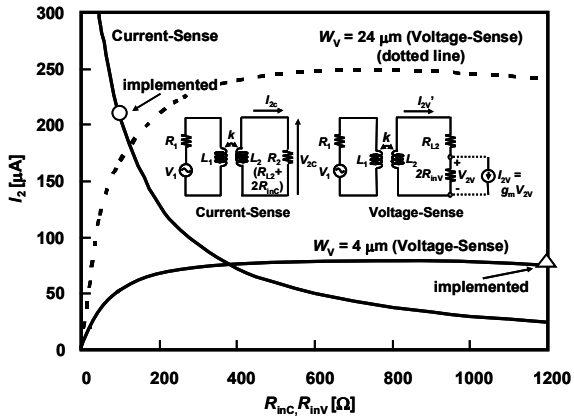

Fig.6 Comparison of topologies of two receiver circuits (R_1=100Ω, R_2=R_{in}+R_{L2}(R_{L2}=120Ω), L_1=0.8nH, L_2=4.2nH, ω=2π∗1.5Grad/s, k=0.28).

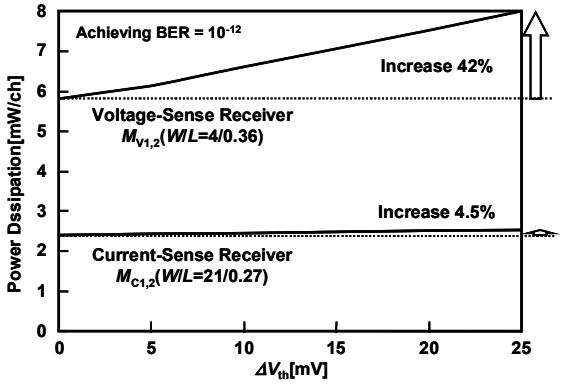

Fig.7 Immunity to variation of threshold voltage.