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A Single-chip Ultra-Wideband Receiver using Silicon Integrated Antennas for Inter-chip Wireless Interconnection

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1. Introduction

Wireless interconnections among ULSI chips have a possibility of 3-dimensional mounting on print-circuit board (PCB). Clock and data are transmitted without bonding wires and printed metal patterns. Recently, 3-dimensional custom stacked system (3DCSS) has been proposed [1]. 3DCSS has local wireless interconnections (LWI) using spiral inductors, and global wireless interconnections (GWI) using integrated antennas [2]. The target distance of GWI is from a few hundred μm to 1cm, and the first target of bit error rate (BER) is < 10^{-5} without error correction. Pulse-based ultra-wideband (UWB)[3] is adopted as a communication method of GWI, where the Gaussian monocycle pulse (GMP) is generated by simple logic operations [4]. In the receiver side, simple circuitry is possible when on-off keying (OOK) modulation is adopted. In this paper, UWB-OOK method for such a short distance communication is studied. HSPICE simulations of UWB-OOK clock/data receivers are carried out, and jitter characteristics of recovered clock are investigated.

2. Circuit design

Figure 1 shows block diagram of OOK-UWB clock and data receivers. Here, the integrated antenna is directly connected to the differential amplifier (Fig. 2 (a)) without impedance matching. Received GMP is amplified and given as an input of double balanced mixer (Fig. 2 (b)). The mixer outputs the square of GMP. After amplification and differential/single-ended conversion using current mirror circuit (Fig. 2 (c)), the signal is given as an input of buffer via AC coupling. Inverter buffer performs A/D conversion, thus it outputs rectangular pulses. In this method, recovered data is not non-return zero (NRZ), but return zero (RZ). D-flip-flop (D-FF) performs RZ/NRZ conversion. The recovered clock is delayed and its rising edge is used as a trigger of D-FF. Figure 3 shows a layout of UWB-OOK receiver. The receiver circuit design has been done by TSMC 0.18-μm mixed signal design rule.

3. Results

The performances of the current OOK-UWB clock/data receivers are shown in Table 1. UWB-OOK transmitter generates GMP of 1 Gbps / 250 Mbps clock/data. Figure 4 shows a schematic cross sectional view of 3DCSS, which is composed of PCB (FR-4), stacked silicon chips with integrated dipole antennas and flexible printed circuits (FPC). 6-chip-stacked module was simulated using MW-STUDIO, and calculated 2-port S-parameters were shown in Fig. 5. Here, the antenna on the bottom silicon is called as port 1, and that on the top silicon is port 6. EMtoSPICE converts S-parameter to the spice netlists of equivalent circuits.

Figs. 6 (a) and 6 (b) are transmitted 250 MHz GMP clocks from port 1, and received GMP at port 4, respectively. Figure 6 (d) shows that the receiver succeeded in recovering the clock, which has the same cycle as that of the internal oscillator in the transmitter (Fig. 6 (c)). It also shows that the rectangular pulse width is different. In the present application, the only rising edge is used as the trigger signal. The analogous results at 1 GHz are shown in Fig 7. Figure 8 shows data recovery at 250 Mbps. However, 1 Gbps data recovery causes error due to inter-symbol interference (ISI), because the center frequency of the received GMP is almost 1GHz.

Figure 9 shows probability distributions of recovered 250MHz clock for (a) period T, (b) pulse width PW and (c) rising time t_{rise}. The definition of jitter is given as the standard deviation of the Gaussian distributions. In Fig. 10, the ratios of jitters to averages of T, PW and t_{rise} are plotted as a function of distance. Jitters of PW are 3.1-17.3% at 1 GHz and 3.7-7.9% at 250 MHz. Figure 11 is the probability distribution of PW at 250 MHz for port 6. It shows a specific behavior when the non-Gaussian deterministic jitter (Dj) becomes more dominant than random jitter (Rj). The large values of σ_{PW} are related to the asymmetrically long tail of GMP, the frequency characteristics of the whole system causes such tail. Thus, this type of Dj is classified into ISI, which will be improved by the assurance of enough bandwidth. Rj is dominant without ISI.

Period jitter is important for RZ/NRZ conversion, and its values are 1.1-3.1% at 1 GHz and 0.4-1.9% at 250 MHz. The data also have almost the same period jitter. The average delay of clock compared to data is τ = 647 ps ≈ T/6, and error occurs when the clock comes faster than data, thus the timing error probability P_t is calculated as follows.

$$P_t = \sum_{i=1}^{n}\sum_{j<i} P_{dat}(t_i)P_{clk}(t_j-\tau) \Big/ \sum_{i=1}^{n}\sum_{j=1}^{n} P_{dat}(t_i)P_{clk}(t_j-\tau) \quad (1)$$

Here P_{dat} and P_{clk} show probability distributions of T for RZ data and clock. Estimated P_t are shown in Fig. 12, and the value is $2.85\text{x}10^{-10}$ for port 6. Figure 12 also shows that the limit of the distance to realize $P_t < 10^{-5}$ is 0.707mm.

4. Conclusion

OOK-UWB clock and data receivers based on 0.18-μm CMOS process have been developed. The receivers could recover 1GHz/250MHz clocks and 250MHz data successfully. Calculated RZ/NRZ conversion error P_t is $2.85\text{x}10^{-10}$ for port 6, and longest distance to realize $P_t < 10^{-5}$ is 0.707mm.

Acknowledgements

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References

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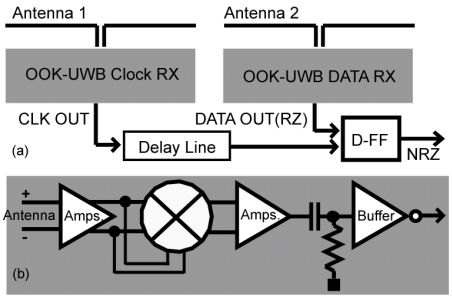

Fig. 1 (a) OOK-UWB clock/data receivers. (b) Block diagram of OOK-UWB receiver.

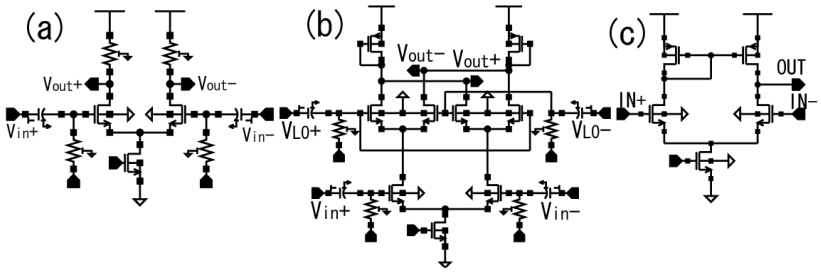

Fig. 2 Schematic diagrams of UWB receiver. (a) Differential Amplifier. (b) Mixer. (c) Current mirror circuit.

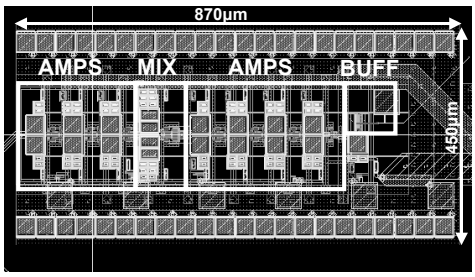

Fig.3. Layout of UWB-OOK receiver.

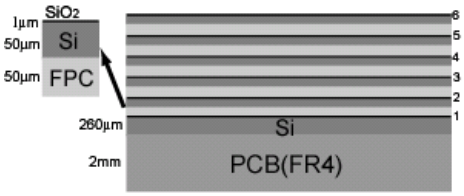

Fig. 4. Cross sectional view of 3DCSS structure.

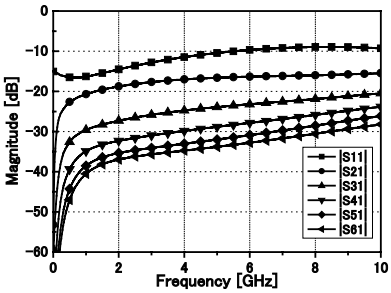

Fig.5. Calculated S-parameters of 3DCSS system.

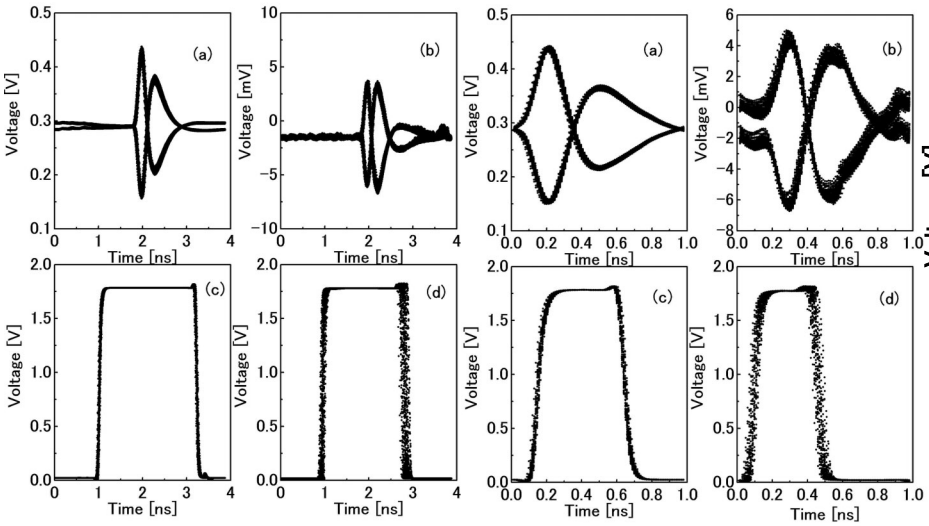

Fig.6. 250MHz clock recovery. (a) Tx (port 1) output. (b) Rx (port 4) input . (c) VCO (in Tx) output. (d) Rx output.

Fig.7. 1GHz clock recovery. (a) Tx (port 1) output. (b) Rx (port 4) input . (c) VCO (in Tx) output. (d) Rx output.

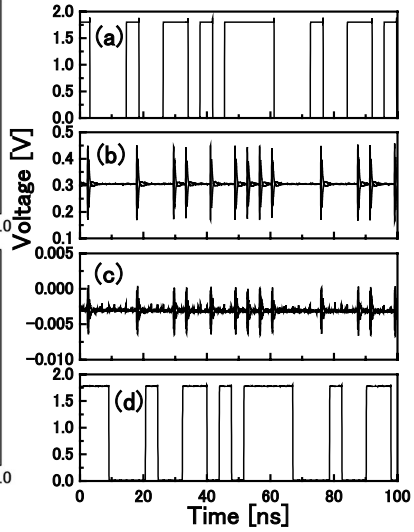

Fig.8. 250Mbps data recovery. (a) Data input. (b) Tx (port 1) output. (c) Rx (port 6) input. (d) Data output.

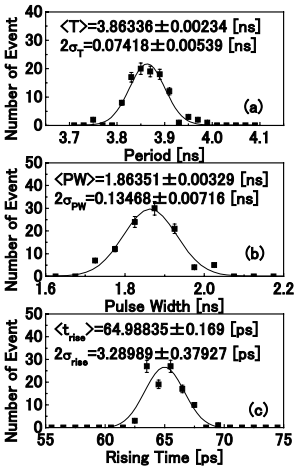

Fig. 9 Jitter distribution of recovered 250MHz clock (port 4). (a). Period. (b) Pulse width. (c) Rising time.

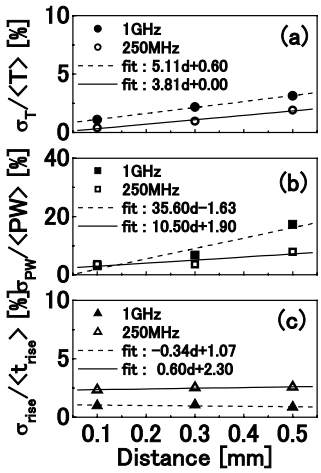

Fig. 10. The ratios of jitters to averages. (a). Period. (b) Pulse width. (c) Rising time.

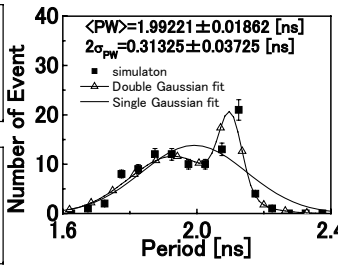

Fig. 11. PW jitter distribution of 250MHz clock (port 6).

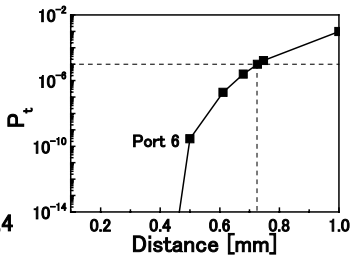

Fig. 12. Timing error probability of RZ/NRZ conversion versus distance.

Technology	TSMC 0.18μm CMOS
Modulation	OOK
Area	0.39mm^2
Power	40mW
Clock	1GHz/250MHz
Data rate	250Mbps

Table 1. Performance of OOK-UWB receiver.