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A 0.18 μm CMOS Impulse Radio Based UWB Transmitter for Global Wireless Interconnections of 3D Stacked-Chip System

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1. Introduction

For future ULSIs, signal integrity of global interconnection will be a critical issue. 3D-intergration called 3D Custom Stacked System (3DCSS) has been proposed for inter-chip communication as shown in Fig.1 (a) [1]. Local wireless interconnection using inductive coupling had been proposed [2]. However it limits transmission distance up to 300μm and the system has no multi-chip accessibility. Therefore, global wireless interconnection has been proposed, which utilizes electromagnetic wave transmission by using integrated antennas and an ultra wideband (UWB) transceiver system [3, 4]. Impulse radio based UWB uses short Gaussian monocycle pulses (GMP) as a transmitted signal. Since the GMP transmission does not require any carrier, we can make transceiver circuits simpler and smaller than heterodyne-based one.

In this work, we developed inter-chip data and clock transmissions for the stacked Si chip structure having on-chip impulse radio based UWB transmitter by use of TSMC 0.18μm CMOS technology. The transmitted signal is differential Gaussian monocycle pulse (DGMP) with data rate of 250Mbps via linear dipole antenna pair which are integrated in different Si chips. On-off-keying (OOK) modulation scheme is adopted.

2. GMP Clock Transmitter

Schematic diagram and layout of clock transmitter are shown in Figs.1 (b) and 3(a). 8-staged voltage controlled ring oscillator (VCO) first provides 1GHz rectangular shaped pulse. The pulse is converted to 250MHz rectangular shaped pulse and generates GMP as a UWB signal at the output of GMP generator. A block diagram of GMP generator is shown in Fig.1 (c). EXOR makes the impulses from the rectangular pulse and delayed, resulting in forming an impulse. Then, the output impulse is differentiated by RC differentiator. Finally GMP as a UWB signal is transferred to single input dual output (SIDO) amplifier. This circuit block amplifies and converts single-ended GMP to differential GMP (DGMP). Driver amplifier further amplifies the DGMP. Source follower circuits are used to avoid reflection due to impedance mismatch between the driver amplifier output and transmitting antenna (TA). Thus DGMP having clock information is transmitted by integrated dipole antenna (as shown in Fig.4). The center frequency (f_c) of transmitted GMP is 1GHz, peak-to peak voltage is approximately 349mV.

3. OOK Modulated Data Transmitter

Schematic diagram and layout of data transmitter are shown in Figs.1 (b) and 3 (b). Since OOK modulation circuit is composed only D-Flip-Flop (DFF) and AND gate as shown in Fig.1 (b), it occupies very small area. Requirements of modulated signals are 250MHz clock and Non-Return-Zero (NRZ) data signal with the same frequency. Clock is provided from the VCO in the clock transmitter on the same chip. Data which are sent from the other circuits are synchronized with the clock by DFF. When data signal is high level indicates data 1 AND gate generates a rectangular pulse to create GMP. When the data signal is low level, which indicates data 0, no pulse appears. The circuit blocks after AND gate in the data transmitter are the same as in the clock transmitter. Thus OOK modulated UWB signal is transmitted by TA as shown in Fig.5.

4. Driver Amplifier

Inductor-less resistive load differential amplifier, as shown in Fig.2, is used as a driver amplifier because of its small occupied area. To provide large signal amplitude which can reach the furthest receiving antenna, the amplifier has 2 stages. The gain of the amplifier is shown in Fig.6. f_c of amplified GMP is shifted from 2GHz to 1GHz after amplified because of the gain frequency characteristic (17dB at 2GHz, and 22dB at 1GHz).

5. Signal Transmission in Inter Stacked Chips

Signal transmission between antennas on the stacked Si chips is investigated. A transmitting antenna is integrated in a top chip, while receiving antennas are integrated in the lower chips. Simulation results of transmitted and received GMP waveforms are shown in Fig.7. Channel distances are shorter than $\lambda/2\pi$ (where λ is wavelength), so this implementation is in the near field. Peak-to-peak voltages of each GMP and f_c are shown in Fig.8. High-pass characteristics of the channels improve symmetric property of the received GMP and shift center f_c of GMP from 1GHz to 1.24GHz as shown in Fig.7 and Fig.8.

Inter-chip data communication is confirmed as shown in Fig.9. Fig.9 (a) shows 250Mbps OOK modulated GMP which is transmitted from data TA (port7). Received GMP at port12 which is the furthest data RA is shown in Fig.9 (b). Peak to peak voltage of the received GMP is approximately 5.1mV.

6. Conclusion

The GMP clock and OOK modulated data transmitters are developed by use of 0.18μm CMOS technology with 1.8V power supply. Inter-chip clock signal at 250MHz and data transmission with 250Mbps through 6 stacked Si chip are confirmed.

Acknowledgements

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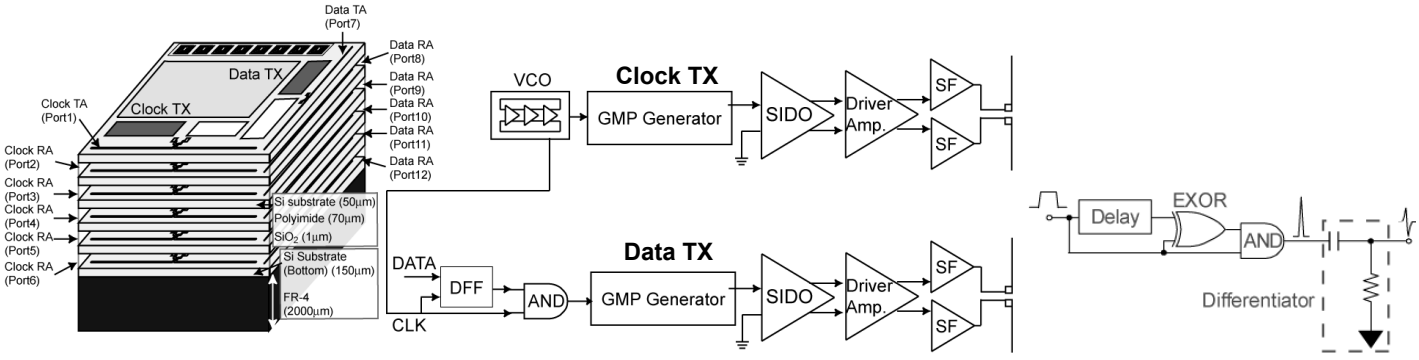


Fig.1 (a) Schematic diagram of 3DCSS structure. Clock and data transmitting antennas are integrated.(b) Block diagrams of clock and data transmitters. (c) Block diagram of GMP generator.

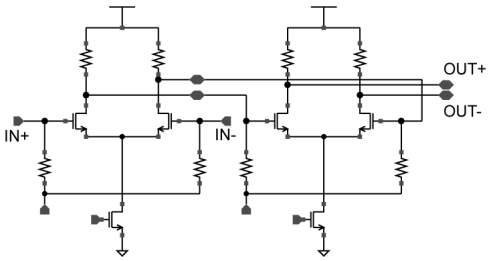
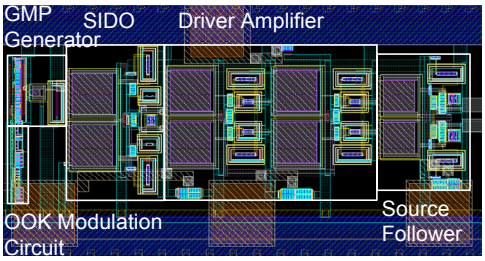
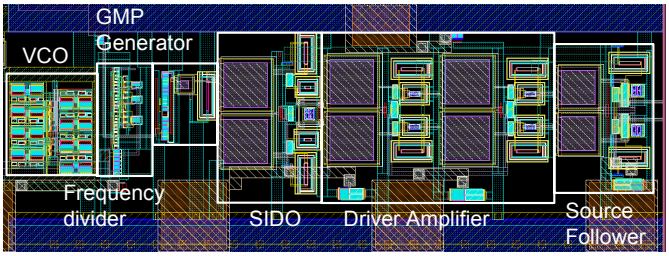


Fig.2 Schematic diagram of driver amplifier.



(a)



(b)

Fig.3 (a) Layout of data transmitter. (b) Layout of clock transmitter.

Table.1 Performance of Clock and Data transmitter Circuits

	Clock transmitter (Data transmitter)
Technology	0.18μm CMOS
Pulse repetition Data rate	250MHz (250Mbps)
Pulse width	1ns
Peak to peak voltage of GMP	349mV
Center frequency of GMP	1GHz
Area	0.163mm² (0.136mm²)
Power Consumption	46mW (36mW)

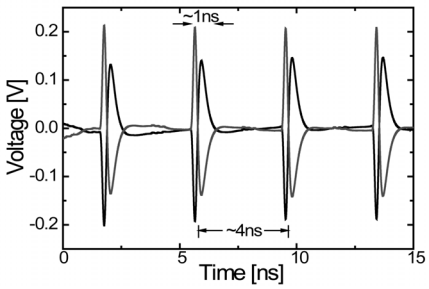


Fig.4 Transient waveform of GMP transmitted by clock transmitter.

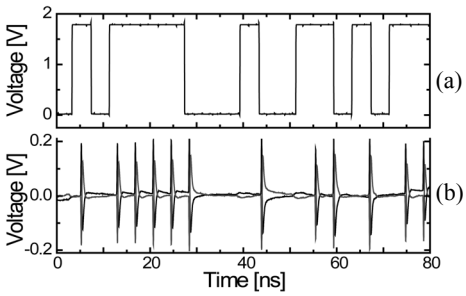


Fig.5 (a) Transient waveform of data input. (b) GMP transmitted by data transmitter.

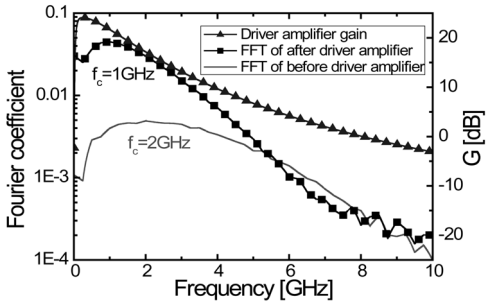


Fig.6 Gain of driver amplifier ,FFT of driver amplifier input GMP and FFT of driver amplifier output GMP.

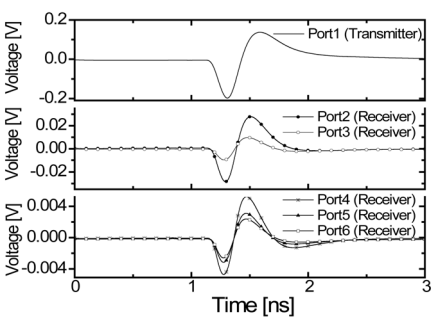


Fig.7 Transient waveforms of GMP Transmitted by Port1and received by each ports. One half of differential signal is only plotted.

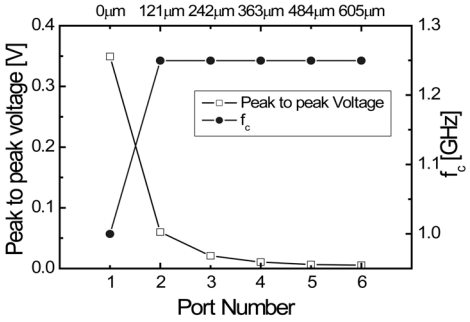


Fig.8 Port dependency of peak to peak voltage of GMP and f_c of GMP. Dependence of distance between a port n (up to 6) to port1 is also.

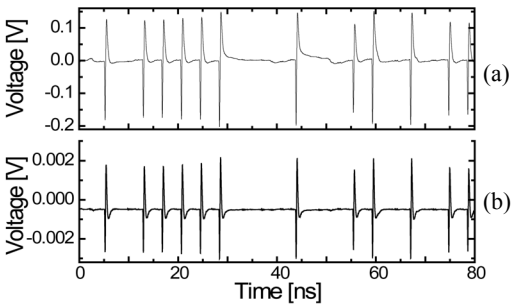


Fig.9 (a) Transmitted waveform of data transmitter. (b) Received OOK modulated GMP at port12.