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Scaling Trends and Mitigation Techniques for Soft Errors in Flip-Flops

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1. Introduction

Soft errors (SEs) induced by secondary cosmic ray neutrons are a significant problem in recent LSIs. Although error correction code (ECC) is easy to apply to RAMs, it is difficult to apply them to logic circuits. SEs in combinational logic circuits (C-Logics) and flip-flops (FFs) are focused on in recent studies [1]. FFs play a major role in SEs in logic circuits in recent technologies. When the scaling trend of SEs is estimated, the timing effect of soft error rates (SERs) in FFs is an important factor for accurate estimations. [2]

In this study we clarify the technology trend of SERs in FFs and discuss SE mitigation techniques. We propose a new SER in an FF (SER_{FF}) model including the timing effect. An SER_{FF} simulation system is constructed based on this model and used to investigate the scaling trend of SER_{FF}. New mitigation techniques based on the model are discussed.

2. Timing Derating Effect of SERs in FFs

We propose an SER_{FF} model including the timing effect which is calculated from a time delay distribution of data paths between FFs. Consider two FFs (FF_1 and FF_2 shown in Fig. 1) connected by a data path with a time delay T_d, which operated with a frequency of $1/T_c$ (T_c: clock cycle time). FF_1 releases error data at time "t" (the rising edge of the clock is assumed to be 0) and the error data propagates to FF_2. When $T_c - t < T_d$, the propagated error data does not affect FF_2 and the FF_2 retention data is not upset (Fig. 1(a)). When T_c-t, > T_d, the FF_2 retention data is upset (Fig. 1(b)).

When error data is released from an FF (FF_1) at time "t", the probability P(t) that the error data is stored in the next FF (FF_2) is

$$P(t) = \int_t^{Tc} D(Tc - T)dT \,, \qquad (1)$$

where T_c is the clock cycle time, and D(T) is the distribution function of the time delay on the paths between connected FFs. D(T) in an LSI chip is calculated with static taming analysis (STA) tool. P(t) means the timing effect in SER_{FF}. The latching rate for the upset data of the next FF (FF_2), $SER_{FF\text{-}real}$, is derived from P(t) as

$$SER_{FF-real} = \frac{1}{T_c}\int_0^{T_c} \{SER_{FF-cell}(t) \times P(t)\}dt \,, \qquad (2)$$

where $SER_{FF\text{-}cell}$ is the rate of the retention data upset in a cell of FF.

Consider SER_{FF} in a 65-nm technology FF(Fig. 2), which has two types of probability distribution functions: $D_a(T)$ and $D_b(T)$ (Fig. 3 (A) and (B)). Figure 4 shows $SER_{FF\text{-}cell}$ simulated in 10-picosecond steps and $SER_{FF\text{-}cell}(t) \times P(t)$ simulated from $D_a(T)$ and $D_b(T)$. At a clock "HIGH", $SER_{FF\text{-}cell}$ dominates $SER_{FF\text{-}real}$. At clock "HIGH", $SER_{FF\text{-}cell}$ is contributed to by the master latch upset. Figure 5(A) and (B) show $SER_{FF\text{-}real\text{-}A}$ and $SER_{FF\text{-}real\text{-}B}$ calculated from $D_a(T)$ and $D_b(T)$. $SER_{FF\text{-}real}$ is 40 to 60% of $SER_{FF\text{-}cell}$. The timing effect enlarges as the D(T) shifts toward T_c ($T < T_c$) .

We have constructed a new SE simulation system for FFs based on this SER_{FF} model. This system is coupled with SE simulator NISES[3], SPICE and STA tool. The charge collection is calculated by the NISES that we developed for estimating the SEs. The critical charge for the error is calculated by SPICE.

3. Discussion

The accuracy of our simulation system is investigated with accelerate experiments with the 90nm technology FF. Figures 6 and 7 show the simulated and experimental SERs. The accelerated experiment has been carried out by using the white neutron beam at the Research Center for Nuclear Physics (RCNP) at Osaka University. This neutron beam is effective for estimating SERs because its energy spectrum is similar to that of atmospheric neutrons at sea-level [4]. The results (Figs. 6 and 7) show good accuracy for the simulations, and the error range is within 40%.

The scaling trends of SER_{FF} are estimated with our simulation system. Figure 8 shows simulated SERs in FFs with 130nm, 90nm and 65nm technology generations. These SERs are almost constant in their SER_{FF} per bit on each technology generation. The SER_{FF} per chip increases as the device density increases. Figure 9 shows the simulated SER in FFs and that for C-logics[5] and SRAMs[4] in 130nm, 90nm and 65nm technology LSI chips(Table 1). If ECC is applied to SRAMs, the SER_{FF} becomes three orders of magnitudes greater than those for SRAMs. These results mean that SEs in FFs are becoming significant.

The following mitigations are proposed based on the SER_{FF} model. Some SE mitigation techniques in latches have been reported [6]. However these techniques force an increase in the FF cell area. These mitigation techniques are effective when applied only to the master latch of FFs following the SERFF model in this paper. As an example, adding 5fF capacitance on the master latch of a 65nm technology FF, decrease the SER by 38% (Fig. 10(i)). Our studies show that it is also effective in controlling D(t). For example, adding some gates on data paths(Fig. 11) to shift D(t) from Fig. 4(A) to (B), decreases the SER by 42% (Fig. 10(ii)). This technique does not decrease the operating speed because the maximum frequency depends on the critical path for which the time delay is the largest. If the both mitigation techniques are applied, the SER decreases by 69% (Fig. 10(iii)).

4. Conclusion

We investigated scaling trends and mitigation techniques for SEs in FFs, and propose an new SER_{FF} model including the timing effect calculated from the time delay distribution of data paths. We constructed a new SER_{FF} simulation system based on the model and investigated the scaling trend of SER_{FF}. SER_{FF} becomes three orders of magnitudes greater than those for an SRAM with ECC, indicating that SEs in FFs are becoming significant. We have also proposed SER_{FF} mitigation techniques based on the model. These techniques are easy to apply and decrease SER_{FF}.

References

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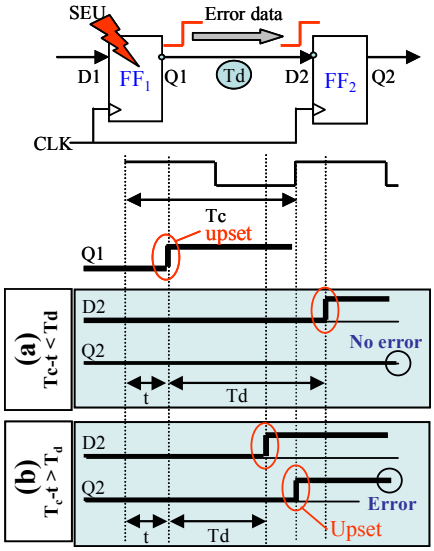

Fig. 1. Timing chart of error data propagation with (a) error and (b) no error.

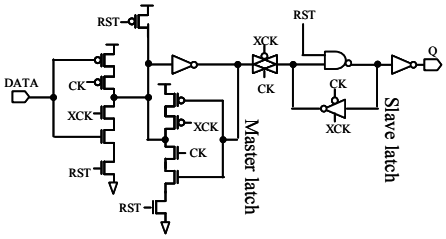

Fig. 2. 65nm technology FF schematic.

Table 1. Simulated chip details

	130nm	90nm	65nm
SRAM	2Mbit	4Mbit	8Mbit
FF	100kbit	200kbit	400kbit
Freq.	500MHz	1GHz	2GHz

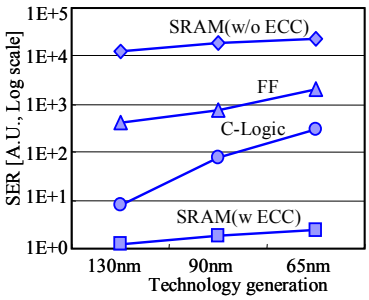

Fig. 9. Simulated SERs in SRAM (with and without ECC), FF and combinational logic for each technology (Table 1).

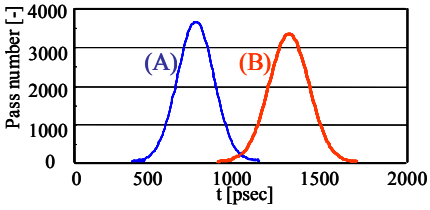

Fig. 3. The distribution of time delays on data passes between an FF and the next FF.

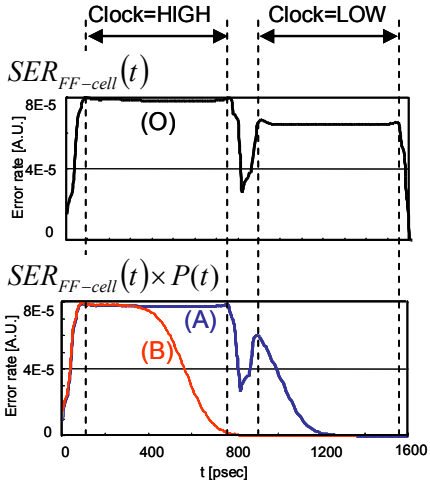

Fig. 4. Simulated (O)$SER_{FF\text{-}cell}$, (A)$SER_{FF\text{-}cell}(t) \times P_A(T)$ and (B)$SER_{FF\text{-}cell}(t) \times P_B(T)$.

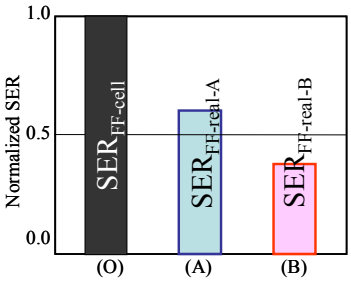

Fig. 5. The normalized SER of the 90nm technology FF, (O)$SER_{FF\text{-}cell}$, (A)$SER_{FF\text{-}real\text{-}A}$ and (B) $SER_{FF\text{-}real\text{-}B}$

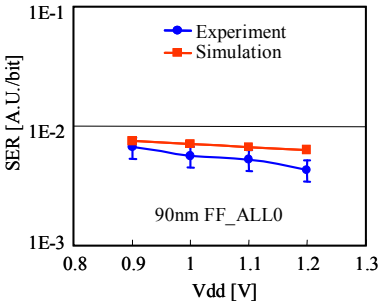

Fig. 6. Experimental and simulated SERs in a 90nm technology FF. All of the data are 0.

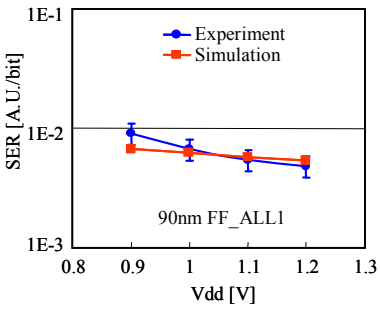

Fig. 7. Experimental and simulated SERs in a 90nm technology FF. All of the data are 1.

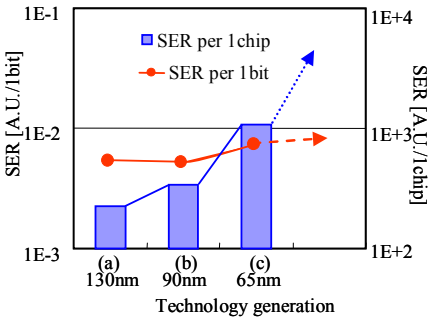

Fig.8. Simulated SERs in (a)130nm, 100kbit, (b)90mn, 200kbit and (c)65nm, 400kbit technology FFs.

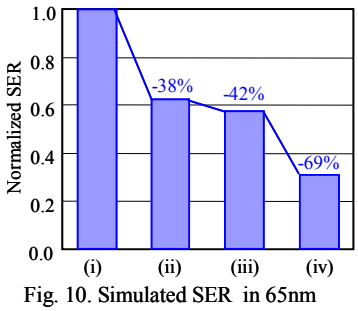

Fig. 10. Simulated SER in 65nm technology FFs with (i) normal, (ii) adding 5fF capacitance, (iii) controlling D(T), (iv) applies to both (ii) and (iii).

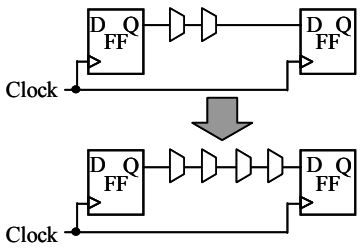

Fig. 11. Adding gates on data passes to shift D(T) .