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SiO_x/β-SiC/Si MIS Resistive Memory Devices Formed by One- and Two-Stage Oxidation of β-SiC

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1. Introduction

We have previously proposed a SiO_x/β-SiC/Si MIS-structured nonvolatile resistive RAM device [1]. The SiO_x layer is formed by oxidation of the β-SiC layer grown on Si(111). A typical *C-V* curve exhibits an injection-type and a donor-type hysteresis, suggesting that injection and ejection of electrons in and out of donor-like states generated near the SiO_x/β-SiC interface relate to the change of the device resistance. With this device, a low-resistive "on" state and a high-resistive "off" state can be used as a "1" and a "0" memory state, respectively.

In this paper, we report a further investigation on the relationships between the oxidation conditions, the oxsides states, the memory characteristics and the memory function mechanisms.

2. Experimental

In Fig. 1, we show the layer structure of the SiO_x/β-SiC/Si resistive memory device. β-SiC layers were formed on 0.1 – 0.5 Ω-cm n-type Si(111) substrates by the chemical vapor deposition method. The oxide layer was formed by thermal oxidation of the β-SiC layer. The oxides were formed by one-stage oxidation at 1000 ºC or by the two-stage oxidation process (the first oxidation at 1200 ºC and the second oxidation at 1000 ºC). After the electrode formation for both the sides of the device, voltages were applied with respect to the Si substrate side.

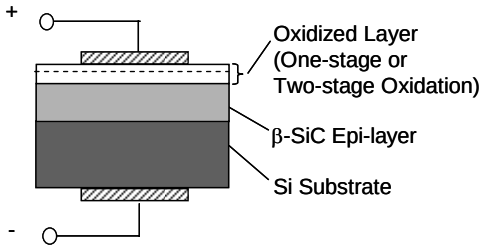

Fig. 1. The layer structure of the SiO_x/β-SiC/Si resistive memory device. The oxide layer was formed by one-stage oxidation or the two-stage oxidation process (see text).

3. Results and Discussion

3-1. Memory behavior of a memory device formed by one-stage oxidation and its memory function mechanisms

A typical *I-V* curve of the memory device formed by oxidation at 1000 ºC is shown in Fig. 2. Clear threshold voltages are observed at which the initial "off" state ((1)) changes to an "on" state ((2)) and the "on" state ((3)) changes to an "off" state ((4)).

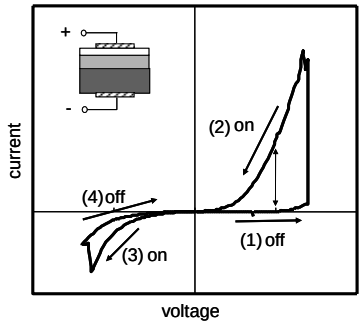

Fig. 2. A typical *I-V* curve of a SiO_x/β-SiC/Si resistive memory device formed by one-stage oxidation at 1000 ºC.

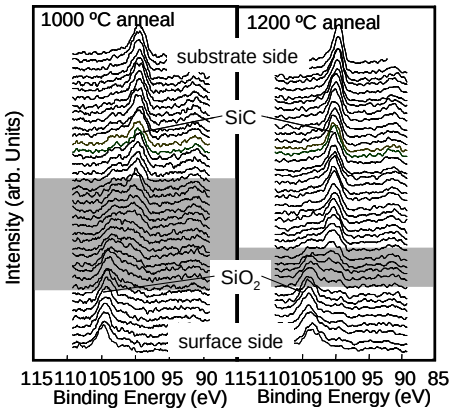

Fig. 3. XPS spectra obtained in the depth direction from SiC layers oxidized at 1000 ºC and 1200 ºC. The gray zones correspond to the imperfect Si oxide interfaces.

When the oxidation temperature (T_{ox}) is 1200 ºC, the hysteresis is very weak. The XPS analyses indicate a SiO_x component and a SiO_x interface region with x being less than 2 are larger at T_{ox} = 1000 ºC than at T_{ox} = 1200 ºC as shown in Fig. 3. Together with the *C-V* results indicating a donor- and injection-type hysteresis, the results suggest that Si^+ donor-like states generated in the imperfect oxide layer and SiO_x/SiC interface with $x < 2$ are responsible for electron trap states.

The suggested memory function mechanisms are illustrated in Fig. 4. Donor-like states act to flatten the SiC band resulting in that the electric field of the Si oxides becomes high and electrons tunnel easily and the state changes to the

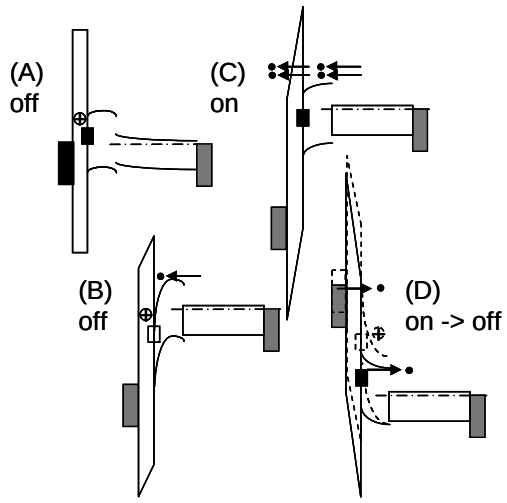

Fig. 4. The suggested memory function mechanisms of the SiO_x/β-SiC/Si resistive memory device.

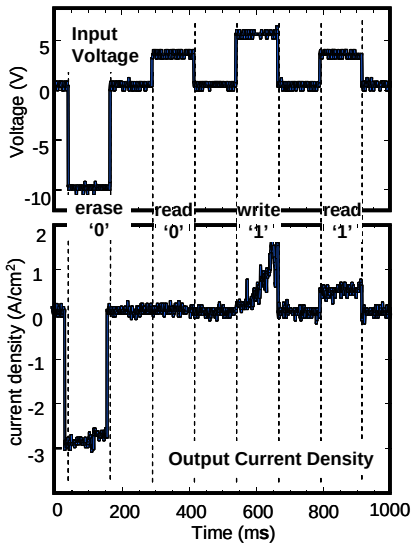

Fig. 5. Typical results of memory function. Input voltages and response currents are shown in the upper and lower figures, respectively.

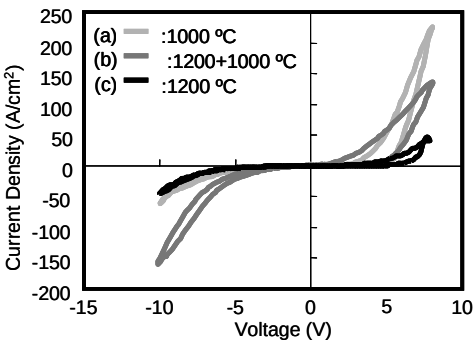

Fig. 6. Typical *I-V* curves of the memory devices formed by oxidation (a) at 1000 ºC, (b) at 1200 ºC and then 1000ºC, (c) at 1200 ºC.

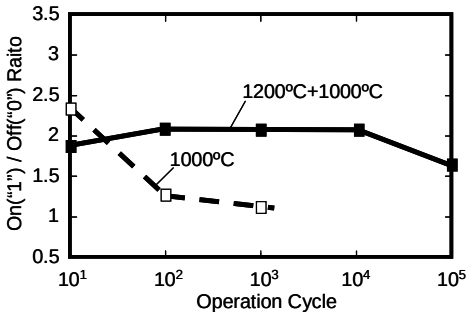

Fig. 7. Dependency of "on" to "off" current ratio on the writing cycle obtained from the SiO_x/β-SiC/Si resistive memory devices formed by one-stage oxidation and the two-stage oxidation process.

"on" state ((B) -> (C)).

In Fig. 5, we show the results of the dynamic response for a "write" operation to switch to the "on" state and an "erase" operation to switch to the "off" state and a "read" operation. The writing and erasing speed are less than 120 μs. An "off" to "on" resistance ratio is more than 10. However, typically, the number of rewriting cycles is in the order of 100 to 1000.

3-2. Improvement of the rewriting cycle by the two-stage oxidation process

As shown in Fig. 3, the oxide layer formed by thermal oxidation at 1000 ºC is imperfect oxide which results in the defect distribution in the entire oxide layer. In this case, some part of the trapped electrons in the "on" state are not easily ejected in the "erase" operation, which degrades the rewriting performance.

Therefore, we have developed the two-stage oxidation method: the first oxidation at 1200 ºC and the second oxidation at 1000 ºC (Fig. 6(b)). The surface-side oxide layer is nearly perfect SiO_2 which has almost no trapping state. The SiC-side oxide layer is imperfect SiO_x with $x < 2$. The SiO_2 layer functions as an electron tunneling layer. The SiO_x and SiO_x/SiC interface have many trapping states. Typically, the SiO_2 and SiO_x layer thicknesses are 12 and 2 nm, respectively. The number of rewriting cycle has improved to be $\sim 10^5$ cycles as shown in Fig. 7. It is considered that the trapping SiO_x layer is designed to be so thin that the trapping electrons can be easily ejected in the "erase" mode.

4. Conclusions

We have previously proposed a SiO_x/β-SiC/Si nonvolatile resistive memory. The donor-like states in the SiO_x play an important role in the memory function. We have further proposed a SiO_2/SiO_x/β-SiC/Si structure formed by two-stage oxidation, which drastically improves the rewriting cycle. This memory is expected to be applied as two terminal nonvolatile RRAM by further process optimization.

Reference

[1] K. Takada, M. Fukumoto, Y. Suda, Ext. Abs. Int. Conf. on Solid State Devices and Materials (Tokyo, 1999) pp.132-133.