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Future Outlook of Floating Gate Flash Memory

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Introduction

The NAND Flash memory has been grown for solid-state mass storage applications. Recently, with the wide spread of the portable equipments, such as digital still cameras, mobile phones and mobile audio fields, the demand for mass-storage and low-cost flash memories has been increased. Therefore, it is indispensable to reduce the cell size and bit cost. To perform low cost and high-density flash memory, Toshiba has been developing Multi-level cells (MLC). In this paper, I will review the critical barriers in future scaling down of NAND Flash. Then, key technologies for breakthrough the barriers will be discussed.

Cell scaling barrier

Fig.1 shows the cross-sectional view of the Floating Gate (FG) memory cell in the 90nm node and beyond. Fig.2 shows TEM cross-sectional view of the 90nm node memory cell [1]. In Fig.1, typical MONOS cell is compared to the FG cell. The main difference between both cell is listed in table 1. One of most characteristic features of MONOS cells is programming operation using direct tunneling current, which is possible due to very thin tunneling Oxide. Recently, novel MONOS cells, which utilize a high-k dielectric thin file for top barrier, are reported (for example [2]). By improving top barrier characteristics, the wide Vth window for the MLC is achieved.

As Fig.1 shows, FG is completely self-aligned to active area. The coupling ratio between control gate (CG) and FG is obtained by inter-poly ONO layer, covering the top and sidewall of the FG. The other hand, uncovered sidewall of the FG is weakly coupled between adjacent FG-FG, as illustrated in Fig.1. In the programming operation, the Vth of the FG cell is verified to finish the programming. Then adjacent cells are programmed form erase state to program state. Therefore, the verified Vth of last FG cell is modulated as shown in Fig. 3. As the design rule becomes small, the Vth modulation grows influentially.

To overcome the FG-FG coupling noise, it is important to reduce the FG thickness. Fig. 4 shows the dependence of the Vth modulation to the FG thickness [3]. As the FG become thinner, the Vth modulation goes to be smaller. In order to reduce the FG thickness, development of the FG material and fabrication processes is needed. Especially, using the high-k dielectric material for Inter-poly Si thin film is effective, as well as MONOS cells.

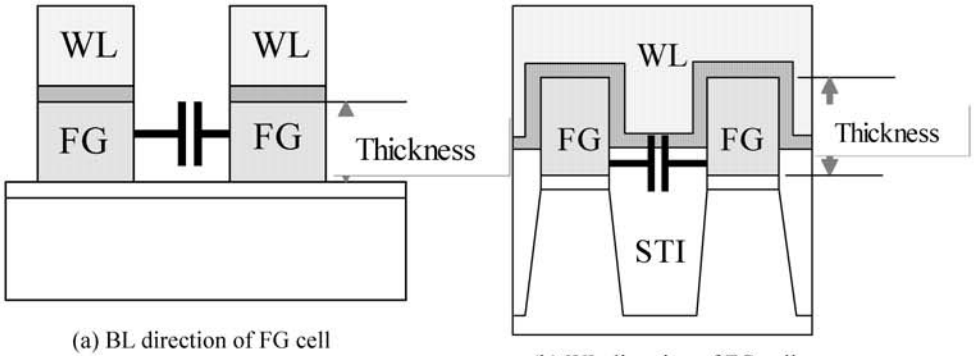
Fig. 5 shows the stored electron number in the FG cell, which is estimated as a function of technology node. The electron number is decreased, as the FG cell size scaling down. For example, FG MLC of beyond 35nm node has only less than 50 electrons. In such a few electron devices, control of the electron location is important. The imbalance location of the electron causes Vth distribution of the memory cells. Fig. 6 shows the electron location of FG cell during program and read operation. The electrons are re-located uniformly due to Coulomb interaction. Because FG, usually fabricated by n-doped poly Si, has about 1e20 donor site per 1cm3, it is enough amount of donor site to relax the imbalance of the electron location quickly. And so, no Vth modulation is occurred due to the location shift of the electrons. It is a large advantage of FG MLC for further scaling down beyond 40nm. Fig. 7 shows the trend of the NAND Flash scaling.

Conclusion

FG type NAND Flash cell has some scaling barrier. In spite of that, it also has large advantage for MLC. The key technology to overcome the scaling barrier is development of novel material for inter poly dielectric film and FG. The NAND Flash memory will surely realize MLC beyond 40nm technology node with FG.

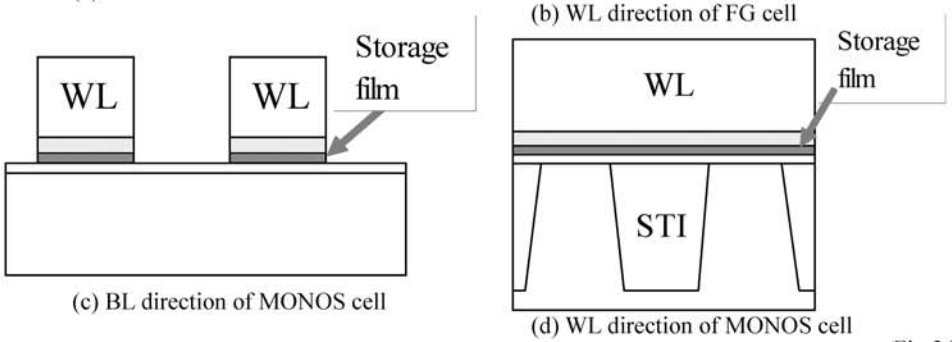
References

[1] M. Ichige, et al.: Symp. on VLSI Tech., pp.89, 2003.
[2] C. H. Lee, et al.: Symp. on VLSI Tech., pp.26, 2006.
[3] R. Shirota: Proc. SSDM 2004, pp.250, 2004.



(a) BL direction of FG cell

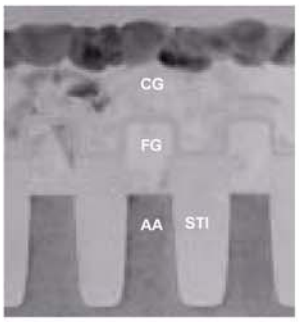
(b) WL direction of FG cell



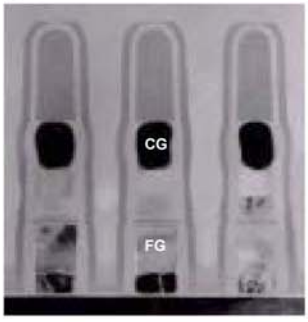
(c) BL direction of MONOS cell

(d) WL direction of MONOS cell

Fig.1 The cross sectional schematic of the FG cell (a)(b). (c)(d) is typical MONOS cell.



(a) Word-Line direction.



(b) Bit-Line direction.

Fig.2 The cross sectional TEM of the FG cell.

	FG cell	MONOS
Storage node	poly Si	(ex.) SiN
Tunnel film thickness	7-9nm	3-5nm
Inter gate dielectric	ONO/high-k	none
Top barrier thickness	none	near 10nm
Program current	F-N	Direct tunnel

Table.1 The mainly difference between FG and MONOS.

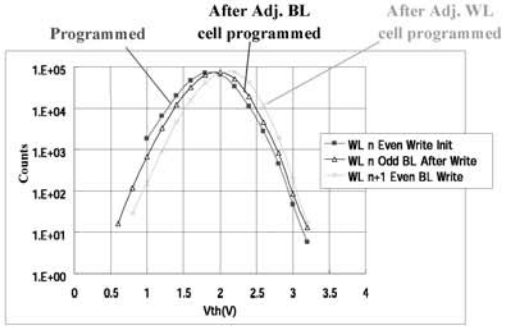


Fig.3 The Vth modulation due to FG-FG coupling noise.

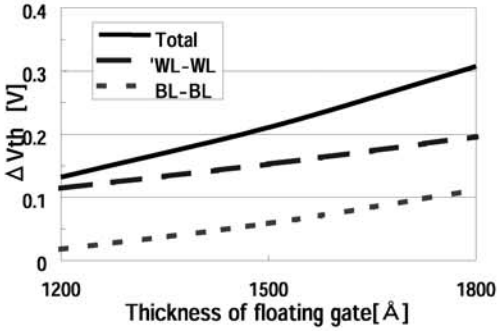


Fig4 The Vth floating gate thickness dependence of the Vth modulation

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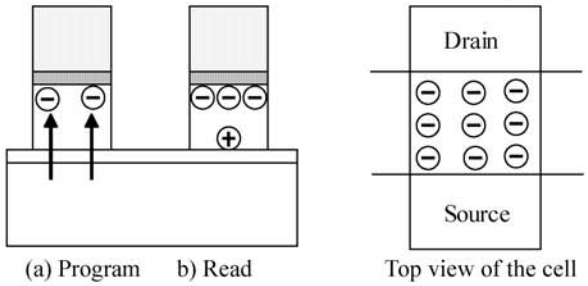

(a) Program b) Read

Top view of the cell

Fig6 The electron location.

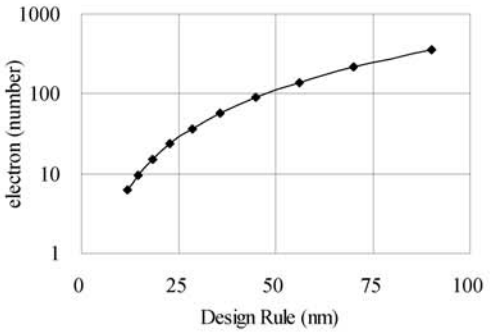

Fig.5. The stored electron number. of FG-MLC

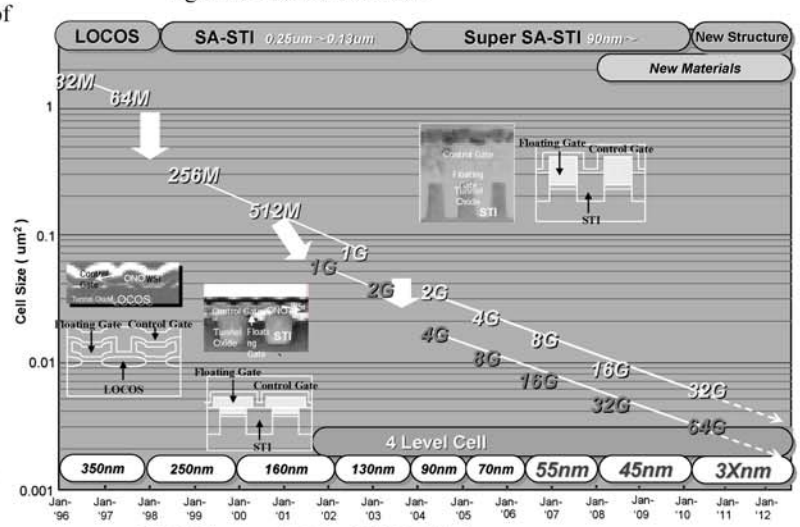

Fig7 The trend of the NAND Flash memory.