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Scalable Wordline Shielding Scheme using Dummy Cell beyond 40nm NAND Flash Memory for Eliminating Abnormal Disturb of Edge Memory Cell

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1. Introduction

For past several years, scaling NAND device has been aggressively achieved to meet ever increasing market demand for high density and low cost NAND flash memory because of explosive growth of portable consumer electronics adopting NAND flash memory such as MP3 music and video players, 3-4G cellular phone, and even notebook computer [1]. As scaling NAND flash device, however, area overhead of two select transistors for NAND string is dramatically increasing due to required punch-through immunity for program inhibition so that it is one of scaling obstacle for NAND flash [2]. Beside that, area of space (*Se*) between select transistor and edge WLs (WL[0, 31]) is another scaling burden, as shown in Fig.1. Reducing the space, *Se* as same as the minimum feature size *F* is hard to be accomplished because of the following two major reasons. One is that increasing capacitive coupling noise between the select transistor and edge WLs as reducing Se. A boosted channel potential of program inhibited memory cell is decreased by a leakage current through select transistor which is slightly turned on when Vpass and Vpgm voltages are applied to the edge WL at *t3* and *t4*, as shown in Fig.2. It results in program inhibition failure. Second reason is that hot-carrier disturbance due to large electric field generated at junction between select transistor and edge WL, as shown in Fig.3. The hot-carrier generation is further enhanced by GIDL current at source/drain of select transistor, as shown in Fig.3 (a), so that at least a larger than 110nm *Se* is required to avoid severe program disturbance [3]. A different environment for edge WL in terms of structure causes also to abnormal electrical characteristics such as erase and program characteristics, as compared to other WLs. It is because that coupling ratio of floating gate is different between edge WLs and other WLs for each operation conditions. It eventually results in wide Vth distributions of erase and program state, as shown in Fig.4. To overcome the scaling issue and electrical effects of edge WL described above, we proposed NAND flash memory with dummy cell and optimized operation conditions in this paper.

2. NAND Flash with Dummy Cell and its Optimized Operation Condition

Fig.5 shows a structure of proposed NAND flash memory with dummy cell. Basically, a dummy cell which is identical to the memory cell is additionally placed between each the select transistors and the edge WLs. The space between the select transistor and the dummy cell is formed by *F*. By adopting these structures and adjusting Vth of the dummy cell combined with optimized bias condition, almost equal environment of other WLs can be provided to the edge WLs so that the undesired edge WL effects can be eliminated. A new program timing diagram for the proposed NAND flash memory is illustrated in Fig.6. It is noted that the dummy cell is used for WL shielding against coupling noise. Before applying Vcc to SSL for precharging channel potential of inhibited NAND string at *t2*, an optimized voltage is applied to the dummy WLs in advance at *t1*. When Vpass is applied to all memory WLs at *t3* and Vpgm is applied to a selected WL at *t4*, the dummy WL works as WL shielding for select transistors against coupling noise from WL[0, 31]. Thus, a bounce of gate voltage of GSL by the capacitive coupling can be suppressed so that the boosted channel potential of program inhibit cell can be maintained. As scaling NAND flash memory below 55nm node, however, the size of NAND flash string with dummy cell starts to become smaller than that of conventional NAND flash string, as shown in Fig.7. It is because that the space between select transistor and edge WL in conventional NAND flash string becomes larger than *3F* including the dummy cell and two space under 55nm node.

3. Results and Discussion

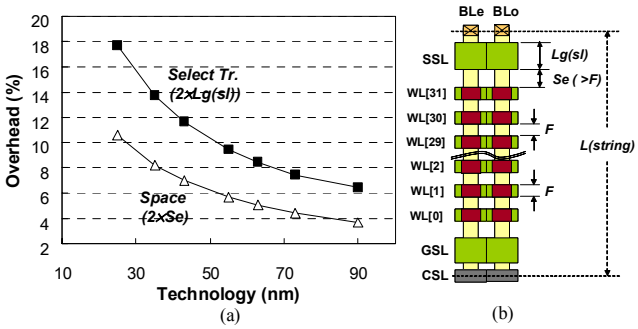
Fig.3 and 8 show a simulated band-to-band generation contour and simulated GIDL field generated at edge WL of the conventional and the proposed NAND at program inhibition condition, respectively. Compared to a large GIDL field which is able to create band-to-band carrier in the conventional NAND, a suppressed low electric field is generated in the proposed NAND due to the dummy cell. It can be explained by that an optimized biased voltage and adjusted Vth of the dummy cell reduce electrostatic potential difference between dummy cell and edge WLs so that it results in decreasing hot electron carriers enhanced by GIDL. A simulated WL-GSL coupling noise as a function of technology node is shown in Fig.9. In the conventional NAND string which use a fixed wide space, 110nm, the simulated coupling noise occurred at GSL is as low as about 85mV almost constantly regardless of NAND scaling. In the case that the space becomes *F* in the conventional NAND, the coupling noise is increasing too high to be accepted as NAND scaling. The proposed NAND string, however, is able to suppress the coupling noise as below as 50mV even at 20nm node. Fig.10 shows measured program disturbance characteristics of edge WLs in the conventional and proposed NAND fabricated by 63nm NAND flash. As NOP (Number of Partial programming) increasing, a severe program disturbance of edge cell is observed at both low and high Vpass region in conventional NAND. In contrast, the program disturbance of the proposed NAND is largely suppressed. As increasing the biased voltage on dummy cell, the program disturbance decreases linearly as shown in Fig.11. From the result, a high bias voltage like Vpass can be used as optimal bias voltage applied for the dummy gates during programming without any additional generated voltage from charge pump. The proposed NAND is also able to improve Vth distribution of memory cells. Fig.12 shows measured Vth distributions of erase state for each WL in the conventional and the proposed NAND. The erased Vth distribution of edge WLs in the conventional NAND is as higher as 0.5V~1.2V compared to other WLs. It causes to increase Vth distribution of programmed state due to charge coupling disturbance. By using the proposed NAND, the difference of erased Vth distribution between edge WLs and other WLs becomes almost negligible, as shown in Fig.12 (b). It leads to better Vth distribution of programmed state compared to the conventional NAND.

4. Conclusions

A WL shielding scheme using dummy cell in NAND flash memory was proposed to eliminate increasing edge WL effects which cause degradations of program disturbance and Vth distribution as NAND flash scaling beyond sub-40nm. The proposed NAND flash can also achieve NAND string scaling by reducing area overhead of space between select transistor and memory cell compared to conventional NAND flash string.

References

[1] Kinam Kim, IEDM, pp.333, 2005 [2] K.T. Park, et al., VLSI Tech., pp.24, 2006, [3] J.D. Lee, et al., NVSMW, pp.31, 2006



(a) (b)

Fig.1 (a) Area overhead of select transistor and space *Se*, (b) Layout view of conventional NAND flash memory

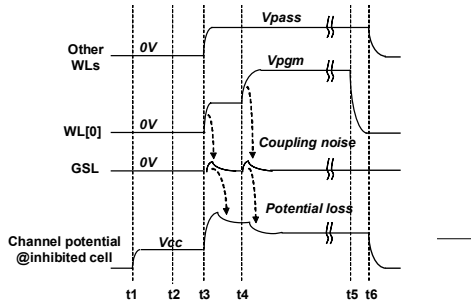
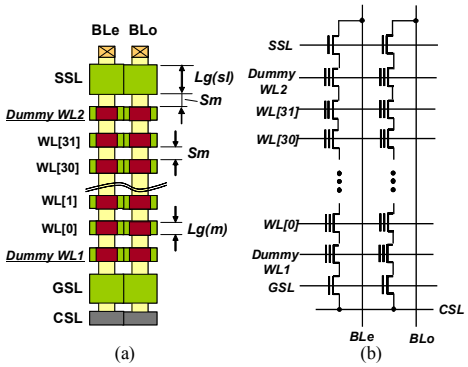


Fig.2 Channel potential loss of program inhibited memory cell due to WL capacitive coupling noise



(a) (b)

Fig.5 Proposed NAND flash, (a) Top layout view, (b) Schematic diagram

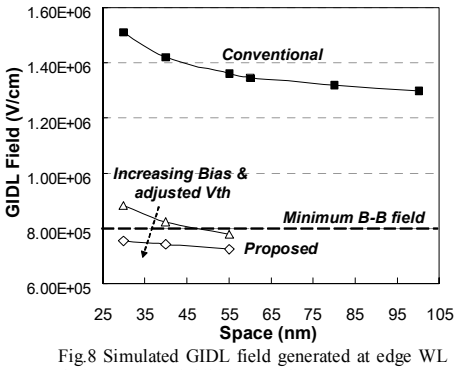


Fig.8 Simulated GIDL field generated at edge WL during program inhibition condition

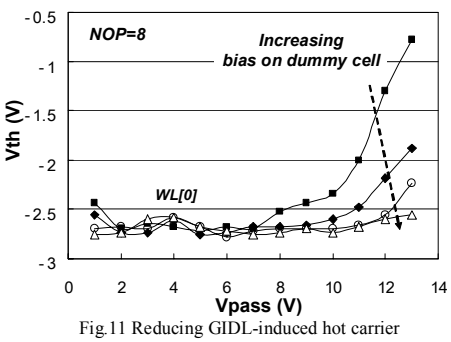
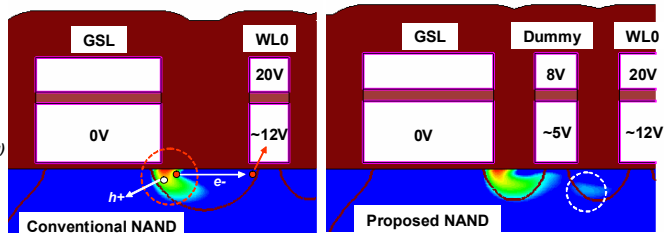
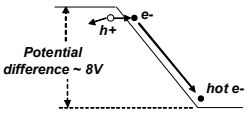


Fig.11 Reducing GIDL-induced hot carrier disturbance by increasing bias voltage



(b) Band-to-band generation contour in proposed NAND



(a) Band-to-band generation contour in conventional NAND

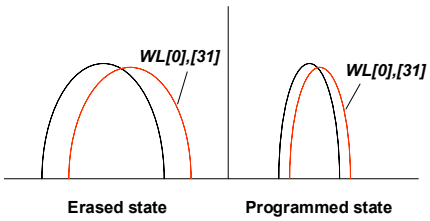
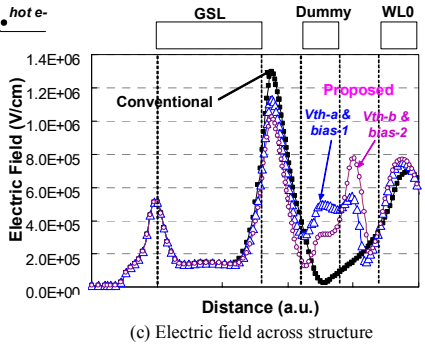


Fig.4 Abnormal Vth distribution of edge WL



(c) Electric field across structure

Fig.3 Simulated band-to-band generation rate and electric field

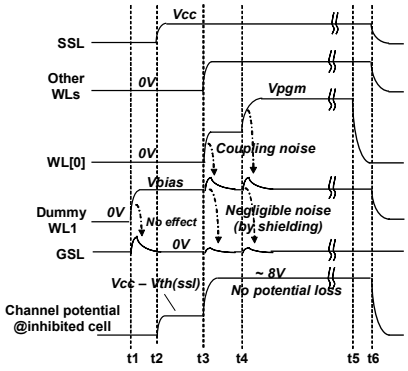


Fig.6 Optimized program pulse timing for the proposed NAND memory

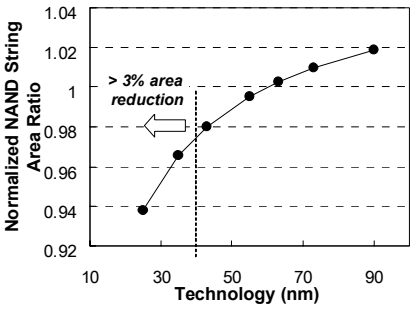


Fig.7 Normalized NAND string area ratio = (Area of the proposed NAND string / Area Of the conventional NAND string) as a function of technology nodes

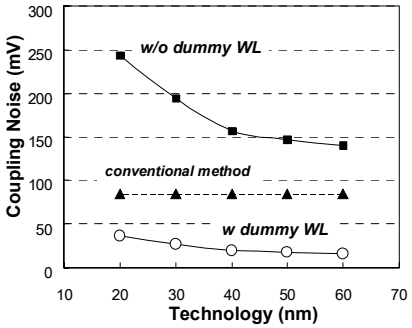


Fig.9 Simulated WL-GSL(SSL) coupling noise comparisons as a function of technology node

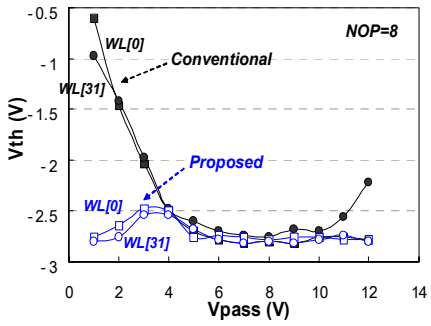
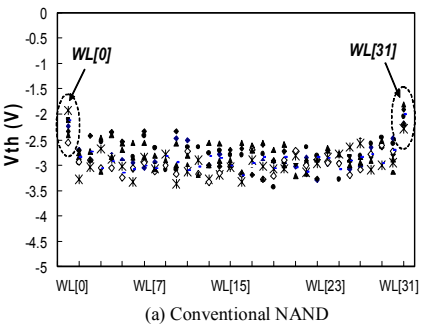
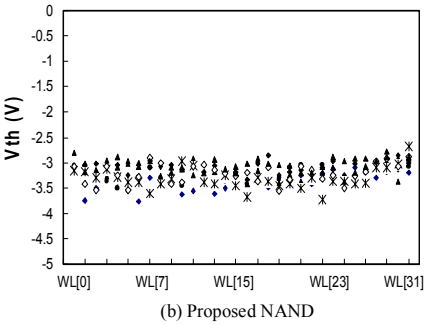


Fig.10 Measured program disturbance of edge WL



(a) Conventional NAND



(b) Proposed NAND

Fig.12 Measured erased Vth of memory cells