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Threshold Voltage Control in Pentacene TFTs by Perfluoropentacene Stack

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1. Introduction

Organic thin film transistors (OTFTs) have been considered to be one of key technologies for realizing flexible electronics. However, unlike many studies on the TFT mobility improvement[1, 2], very little attention has been given to the control of threshold voltage (Vth) in spite of its importance for the practical circuit application. In this study, Vth control in pentacene ($C_{22}H_{14}$) TFTs by stacked perfluoropentacene (PFpen) ($C_{22}F_{14}$) is presented.

2. Concept of Vth Control

Before discussing the way to control Vth, we should understand what determines Vth in OTFTs. We follow Horowitz's idea in which Vth of OTFTs is the gate voltage where the trap carrier density is equal to the free carrier density[3]. Thus, we consider that control of Vth in OTFTs is achieved by changing the number of filled traps.

We propose Vth control in pentacene TFTs by PFpen stack. Expected mechanisms of Vth shift are as follows (**Fig. 1**). (1)Electrons are injected from electrode to PFpen film with no or small bias condition and trapped. (2)The hole injection into pentacene film is induced by those trapped electrons owing to the potential decrease for holes. (3)Traps in pentacene films are filled with those induced holes before operation. In (1), the amount of trapped electrons can be changed by the amount of PFpen stack. By (3), Vth is expected to shift to the lower voltage. The reason we selected PFpen is the lowest unoccupied molecular orbital (LUMO) level of PFpen is almost same as work function of Au, thus electrons injection in (1) is expected[4]. The injected carriers in (1) are expected to be trapped easily because Vth of conventional n-channel PFpen TFTs is higher, which means there are many traps in films. Note that PFpen film should be thin in order for electrode to contact with pentacene film.

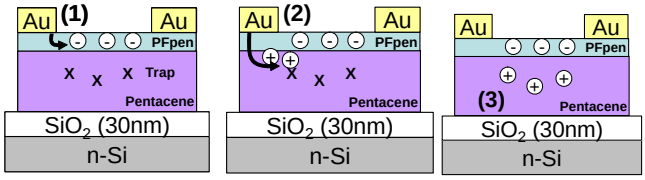

Fig. 1 Schematic cross section of our model. (1)Electrons are injected from electrode to PFpen film and trapped. (2)The hole injection into pentacene film is induced by those trapped electrons owing to the potential decrease for holes. (3)Traps in pentacene films are filled with those induced holes before operation.

3. Experimental Results

We fabricated two types of devices as shown in **Fig. 2**. Pentacene films were deposited on 30nm-thick SiO_2 thermally grown on n-Si substrate. The base pressure was 4×10^{-5}Pa and film thickness was about 50nm. Device (i) is a conventional pentacene TFT and device (ii) is stacked with PFpen on pentacene film. PFpen thickness is 1, 3, 5 and 8nm. Channel width and length are 1000μm and 50μm, respectively.

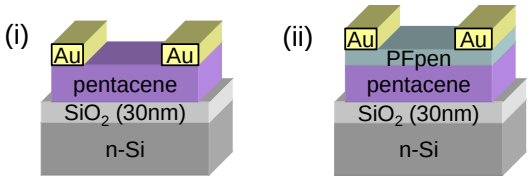

Fig. 2 Schematic structures of fabricated pentacene TFTs stacked with PFpen.

Figure 3 (a) and **(b)** show transfer characteristics and output characteristics of device (i), respectively. The measurements were carried out in dark and vacuum condition. From the transfer characteristic, the mobility is calculated to be 0.23cm^2/Vs using the analytical equation of MOSFETs. We measured transfer characteristics for three times in terms of a concern for stress effect on Vth and no significant change was observed. No sample dependence of Vth was also confirmed. Thus we can discuss a Vth shift though PFpen stack of device (ii) in the following results.

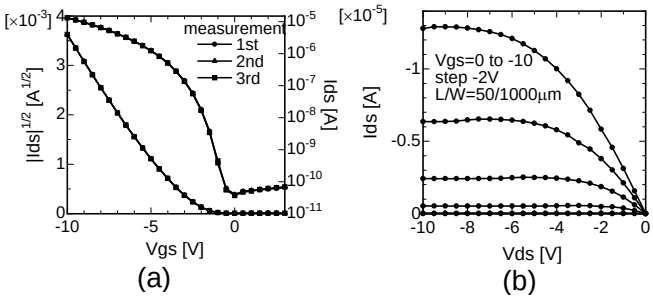

Fig. 3 (a) Transfer characteristics and (b) output characteristics of device (i). The channel length and width are 50 and 1000μm. The mobility and on/off ratio are 0.23cm^2/Vs and 10^5, respectively.

Figure 4 (a) and **(b)** show transfer characteristics change of device (ii) with stacked PFpen thickness. As is discussed, Vth successfully shifts to the lower voltage with an increase of the PFpen thickness. Vth value of -3.2V shifts to -2.6V with PFpen stack of 1nm and -2.2V with that of 3nm, respectively. On the other hand, off current is unfortunately increased and on/off ratio decreases from 10^5 to 10^2 with 8nm stack shown in Fig. 4 (b).

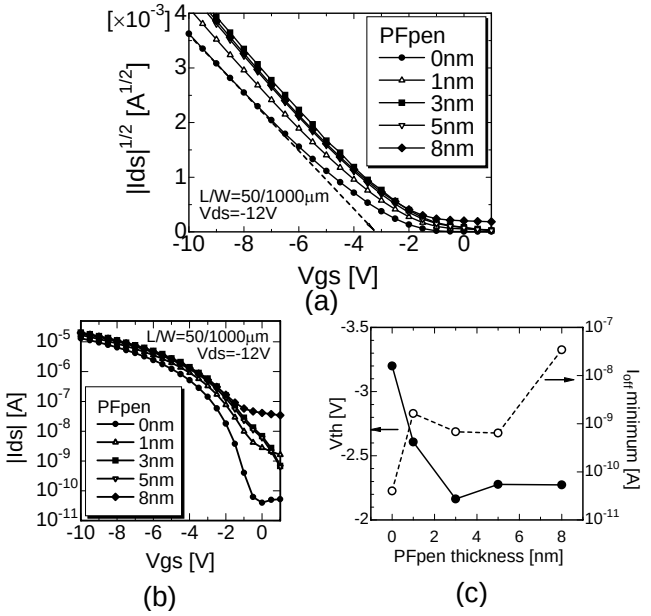

Fig. 4 Transfer characteristics of (a) linear plot and (b) semilogarithmic plot of device (ii). (c) Vth and the minimum value of off current as a function of PFpen thickness.

4. Discussion

To confirm the mechanism of Vth shift, we measured electrical characteristics of device (iii) shown in **Fig. 5**. In contrast to device (ii) in Fig. 2, no change is observed despite 10nm PFpen stack as shown in Fig. 5. This result is quite reasonable with our model. In case of device (iii), electrons cannot be injected into PFpen film because PFpen is deposited on electrodes and crystalinity of PFpen at the edge of electrode is much worse than that on SiO_2 shown in **Fig. 6**. Thus, it is concluded that electron injection is important for the Vth shift.

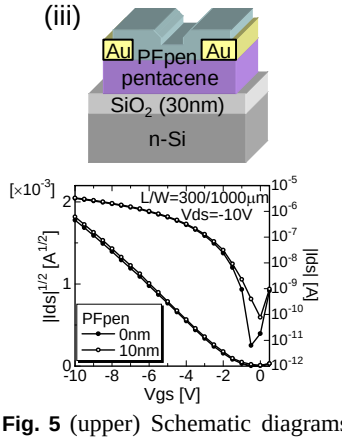

Fig. 5 (upper) Schematic diagrams of device (iii). (lower) Transfer characteristics of device (iii).

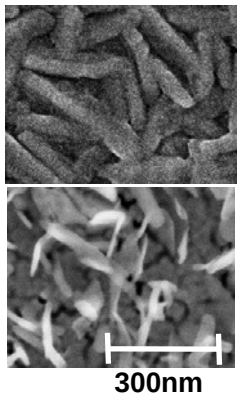

Fig. 6 SEM image of PFpen film on SiO_2 (upper) and Au (lower).

The small increase of off current with PFpen stack under 5nm shown in **Fig. 4 (c)** is considered to be caused by a decrease of pentacene film resistance at the organic interface. In principle, the off resistance of OTFTs operation is achieved by the high resistivity of organic films themselves. Therefore off current increases by PFpen stack because the decrease of resistance is caused by trapped electrons owing to the potential decrease for holes. It is noted that the off current increases abruptly with over 5nm stack of PFpen film. This is because the second channel is formed at organic interfaces. The induced holes are partially trapped, while those partially transfer from source to drain as the off current.

The saturation of Vth shift with over 3nm PFpen stack shown in Fig. 4 (c) may be caused by the decrease of hole injection efficiency due to thicker PFpen film. When stacked PFpen thickness is over 5nm, it seems that Au electrodes don't contact with pentacene film.

Finally, we discuss device (iv) where PFpen is partially stacked shown in **Fig. 7(a)**. **Figure 7 (c)** shows the transfer characteristics change of device (iv). As shown in this figure, Vth shifts to the lower voltage without an increasing of off current. The mechanism of the Vth shift is almost same as one shown in Fig. 1 (1). One difference is that the area of stack is partial. Thus the second channel isn't formed and off condition is achieved by high resistivity of the area without stack shown in **Fig. 7 (b)**. All results well describe our model.

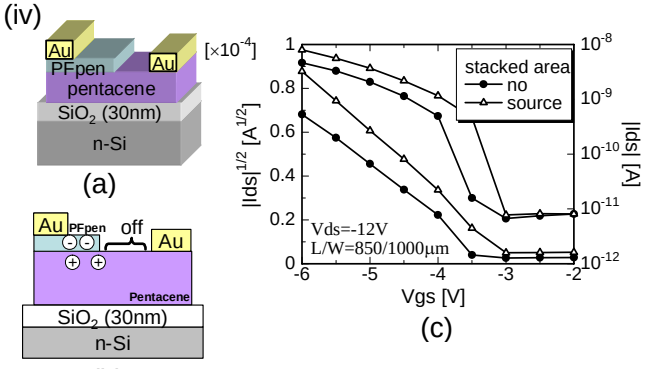

Fig. 7 (a) Schematic diagrams of device (iv). (b) Mechanism of Vth shift without an increase of off current. (c) Transfer characteristics of device (iii)

5. Conclusions

In conclusion, threshold voltage control of pentacene TFTs is demonstrated using PFpen stack. The mechanism is as follows. (1)Electrons are injected from electrode to PFpen film with no or small bias condition and trapped. (2)The hole injection into pentacene film is induced by those trapped electrons owing to the potential decrease for holes. (3)Traps in pentacene films are filled with those induced holes before operation. With under 5nm PFpen film, Vth shift is observed with a small increase of off current. On the other hand, the off current increases abruptly with over 5nm stack because of the formation of the second channel. Following our mechanism, we demonstrate Vth shift without an increase of off current with the device where PFpen is stacked only half channel.

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References

[1] Y. Y. Lin et al., IEEE Electron Device Lett. **18** (1997) 606. [2].H. Klauk et al., Appl. Phys. Lett. **92** (2002) 5259 [3]G. Horowitz and P. Delannoy, J. Appl. Phys. **70**, 416 (1991). [4] T. Yokoyama *et al*., DRC, Santa Barbara, June. 2005.