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Organic Field-Effect Transistor Integrated Circuits using Self-Alignment Process Technology

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1. Introduction

Recently, organic light-emitting diodes (OLEDs) and organic-based field-effect transistors (OFETs) are extensively studied.[1-7] Especially in OFET using pentacene as active layer, highest mobility to date is as high as amorphous silicon (a-Si) FET and this types of OFET will be expected for back plane of active matrix display on flexible substrate. However, in order to obtain higher speed integrated circuit, not only a higher carrier mobility but also reduction of parasitic effect have to be done. In this time, we have investigated integrated circuit that consisted of organic thin-film transistors using self-alignment process technology, [7] and preliminary operation of ring oscillator was confirmed.

2. Fabrication Process of Self-aligned (SA) OFET

Fabrication process of SA-OFET[7] are shown in Fig. 1. First, gate electrode of Ti (100Å)/ Au (1,000 Å)/ Ti (100 Å) is evaporated on fusion-formed aluminosilicate glass (Corning 1737) and patterned using reactive ion etching (RIE). Second, upper layer of titanium was etched off using RIE and gate insulator of Ta_2O_5 (2,000 Å) was deposited using sputtering apparatus. Where, lift-off technique was used for opening a contact hole. Third, back surface exposure was carried out, where the gate electrode was used as a photomask. Ohmic electrode of Cr (80 Å)/ Au (500 Å) was the evaporated and lift-off process was carried out. After finishing lift-off, overlapping length between gate and source/drain electrodes was made as small as 0.5 μm. Therefore, smaller gate capacitance will be achieved. Fourth, after lithographic process was done, the ohmic electrode was etched off using aqua regia and a solution of cerium (IV) diammonium nitride. And then, interconnection of Ti (100 Å) / Al (1,000 Å) was formed using lift-off technique. Finally, the pentacene (500 Å) was evaporated at a substrate temperature of 70℃ in 6×10^{-6} Torr.

A manual prober (Micronics 705A-6) and a parameter analyzer (HP 4155B) were used to measure electrical characteristics. In order to approve superior circuit performance, hand-made circuit simulator was used.[8,9] Figure 2 shows drain voltage vs. drain current characteristics with channel length L of 3 μm. Field-effect mobility (μ_{FE}) of 0.06 cm^2/Vs, on/off ratio of 10^3 and threshold voltage of 0 V were obtained.

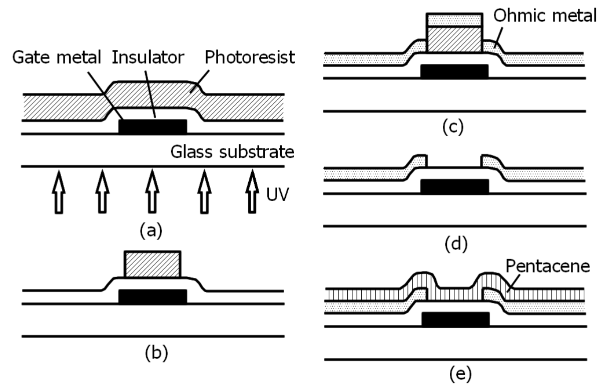

Fig. 1 Fabrication step of SA-OFET.

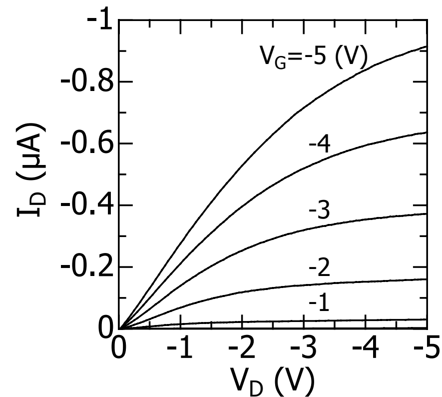

Fig. 2 Drain voltage vs. drain current characteristics.

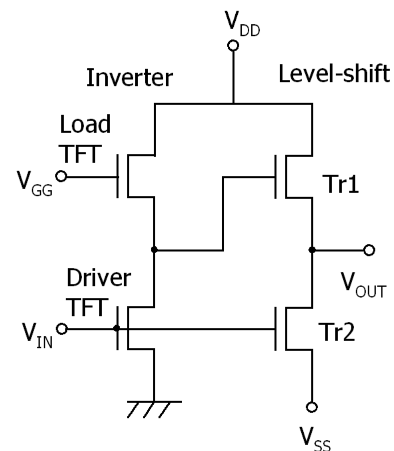

Fig. 3 Developed inverter with level-shift.

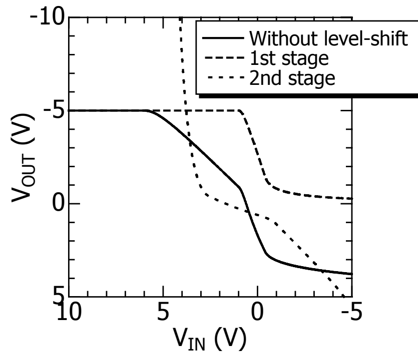

Fig. 4 Transfer curve of inverter with level-shift.

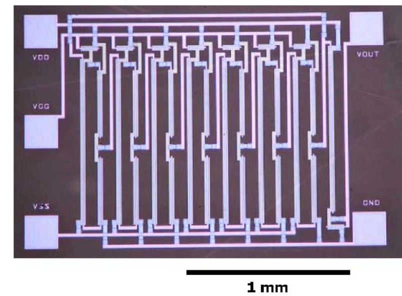

Fig. 5 Photograph of the ring oscillator.

3. Integrated Circuit with pentacene SA-OFET

3.1 Circuit Simulation in Newly Developed Circuit

Figure 3 shows inverter circuit with level-shift under study. A driver transistor at inverter and a gate electrode of level-shift are connected in same wire, *i.e.*, super-buffer configuration is applied to the circuit configuration. In this circuit, shape of transfer curve becomes complex, however, larger gain could be realized by applying antiphase signal into upper and lower level-shift OFET. Therefore, the circuit corresponds to wide margin of input signal. By adjusting a ratio of level-shift circuit as unity, faster carrier injection and extraction could be realized, *i.e.*, faster response is achieved. Gain and logic swing were simulated compared to the previous reported inverter circuit with level-shift, [1,2] where, the threshold voltage of +1.0 V, ratio of inverter of 10, supply voltage V_{DD} of -5 V, level-shift bias V_{SS} of +5 V were fixed and ratio of level-shift circuit was optimized. As a result, the circuit proposed in this time was the most effective with respect to the logic swing and the gain. Figure 4 shows input vs. output voltage characteristics of the circuit, as shown in Fig.3. A wide logic swing of 7.0 V and larger gain of 3.0 were obtained using pentacene SA-OFET with the newly developed circuit configuration.

3.2 Operation of Ring Oscillator

Ring oscillator composed of seven stage level-shift inverters, as shown in Fig.3, and a output buffer. Figures 5 and 6 show photograph of the ring oscillator and obtained oscillation waveform, respectively. Channel length of the pentacene SA-OFET was 9μm, V_{DD} was -5 V and V_{SS} was +5 V. By calculating an oscillation period of 0.34 ms, propagation delay of 24 μs/stage was obtained. Transit time of intrinsic FET was given by $\tau = L^2 / \mu V$. Field-effect mobility of the pentacene SA-OFET was 0.06 cm^2/Vs and channel length was 9 μm. To date, transistor operation with channel length of 3 μm was confirmed and higher mobility was also confirmed.[7] Therefore, the propagation delay of several μs/stage will be realized by miniaturization of the channel length (~1/3) and improvement of the field-effect mobility (~twice).

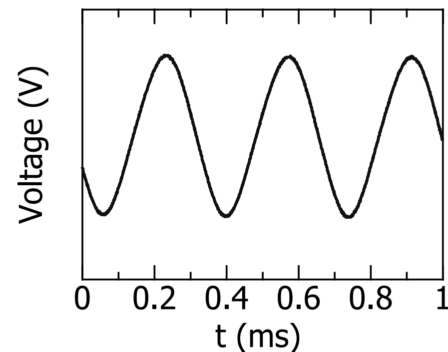

Fig. 6 Measured output waveform of ring oscillator.

4. Conclusions

Ring oscillator composed of level-shift inverter with pentacene SA-OFET was realized for integrated circuit fabrication. For improving the device performance, the propagation delay of several μs/stage will be achieved. By doing this target, not only the back plane of active matrix display, but also the circuit configuration for gate-driven shift register will be expected.

Acknowledgment

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