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Logic circuits with pentacene and ZnO transistors

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1. Introduction

Organic field effect transistors (OFETs) are very attractive device for fabricating the flexible displays, information tags, soft sensors etc. However, organic semiconductors have some disadvantages of low current density and low speed of operation due to their high resistivity and low carrier mobility. Therefore, much work has been devoted to achieving the high field effect mobility and to understanding the operation mechanism of the organic field effect transistors (OFETs) in order to realize the high performance devices. Especially in display, the main application of OFETs in recent reports is related to pixel switches in active-matrix displays but we can show a little other devices in spite of complementary circuits and logic circuits are very important devices for realizing flexible sheet displays. Organic static induction transistor (SIT) with vertical structure has been expected for the high-speed and high-power operation device [1] due to the short channel length than that of lateral type transistor such as metal-oxide-semiconductor transistors (MOSFETs). The excellent characteristics of the organic SIT arise from the very short current pass corresponds to the thickness of an organic semiconductor film between the source and drain electrodes. In addition, to achieve the high on/off ratio and high current values in the OSITs, we have investigated the influence of inserting ultra-thin CuPc layer between the source electrode and pentacene film on the static characteristics of OSITs [2]. These results provided an important fact indicating that a high on/off ratio and a high current value in OSITs are achieved by controlling the interface energy band condition between the organic semiconductor layer and source electrode.

In recent articles, Jackson et al. proposed organic thin-film transistors and integrated circuits using pentacene as the active material [3], Tokito et al. reported CMOS inverter using pentacene as the p-type material and perfluoropentacene as n-type material [4], and Dodabalapur et al. developed hybrid complementary inverters with n-channel a-Si transistors or F_{16}CuPc and p-channel organic transistors [5-6].

In this study, we first briefly describe the transfer characteristics of pentacene SIT inverters, furthermore we demonstrate complementary inverter circuits with p-channel pentacene TFT and n-channel ZnO TFT. These inverters have excellent transfer characteristics and these advantages make useful organic logic circuits for many applications.

2. Experimental procedure

Figure 1 shows a schematic diagram and measurement circuit of a pentacene SIT. Device processing is as follows. First, the ultra-thin CuPc layer of 1 nm was deposited on ITO formed on glass substrate. Second, the pentacene thin

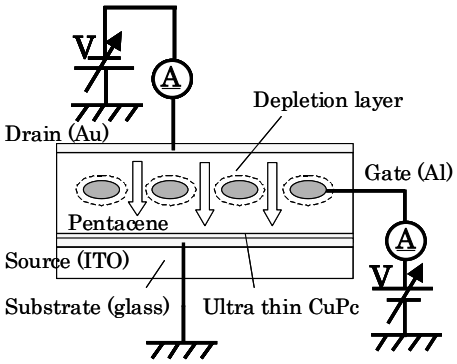

Fig. 1. Schematic diagram of pentacene SIT with ultra-thin CuPc layer on glass substrate.

film of 100 nm was deposited on the CuPc layer. Third, a very thin Al film of 30 nm was formed on the pentacene, a grid type gate electrode with a line and space region was fabricated using an evaporation shadow mask technique. In

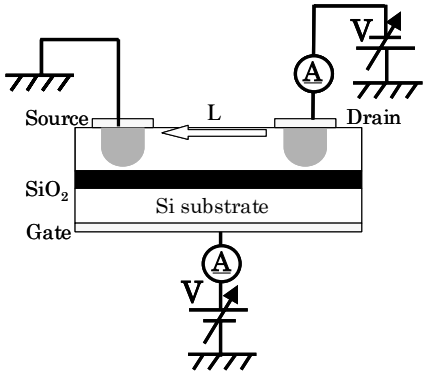

Fig. 2 Schematic diagram of pentacene TFT and ZnO TFT on Si substrate.

this case, the estimated gap between gate electrodes was approximately 4 μ m. Fourth, the Al film as a gate electrode was covered with the pentacene film of 100 nm. Schottky

barrier was formed between the pentacene and Al gate electrode interface. Finally, the drain Au electrode was formed on the pentacene film. The CuPc layer and pentacene films were fabricated under a vacuum of 2×10^{-4} Pa. The source temperatures of CuPc and pentacene were approximately 420℃ and 200℃, respectively. The evaporation rate of organic semiconductors was 0.1nm/s.

Figure 2 shows a schematic diagram and measurement circuit of a pentacene TFT and ZnO TFT, respectively. As shown in Fig. 2, thickness of each layer was 1μm (SiO_2) and back gate electrode of 100nm (Al). The pentacene thin film of 100 nm was deposited on the SiO_2 layer and source and drain-electrode of 150 nm (Au). The channel length of pentacene TFT was 100 μm and channel width 3mm was fabricated. On the other hand, ZnO TFT was fabricated 70 nm (ZnO), source and drain-electrode of 150 nm (Al), and channel length 20 μm and channel width 3mm. ZnO thin film layer was fabricated using radio frequency (RF) sputtering method. RF sputtering equipment (ANELVA L-332S) was used to deposit ZnO.

3. Results and discussion

Figure 3 shows the voltage transfer characteristics of a pentacene SIT inverter based on enhancement-load/ enhancement-drive type layout with a threshold voltage of around –1V. Supplying voltages (V_{DD}) are from –1.2V to –0.8V and from +0.8V to +2.0V step 0.2V, respectively. The circuits show usefully large voltage gain. We can realize a simple voltage inverter by integrating two pentacene SITs in a circuit such that one is acting as a

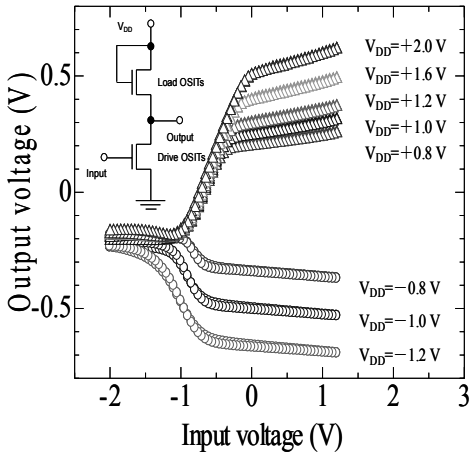

Fig. 3. Schematic diagrams and voltage transfer characteristics of pentacene SIT inverter.

voltage-controlled switch (or driver) and the other is as active load. These transfer characteristics as shown in Fig. 3 are obtained by employing SITs which have a large on/off ratio and high current value. Figure 4 shows the transfer characteristics of complementary inverter combined with a p-channel pentacene TFT and n-channel ZnO TFT. Field–effect mobilities for holes and electrons were approximately 10^{-2} cm^2/Vs and 10^{-3} cm^2/Vs, respectively. These TFTs were electrically connected to form an inverter circuit (See inset in Fig. 4). At a low voltage region (V in), the n-channel ZnO TFT is on state and the p-channel pentacene TFT is off state. Therefore, the output voltage (V out) is high level. On the other hand, at a high voltage

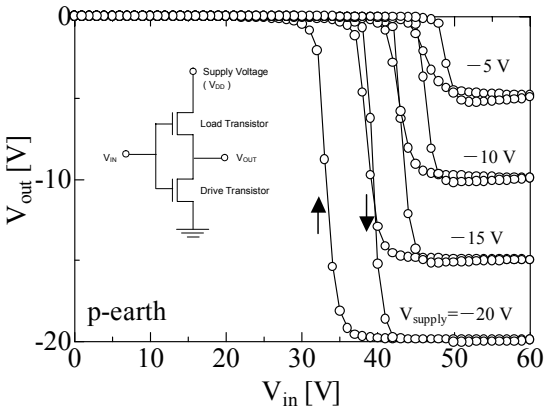

Fig. 4 Transfer characteristics of complementary inverter with p-channel pentacene TFT and n-channel ZnO TFT.

region (V in), the n-channel ZnO TFT is off state and the p-channel pentacene TFT is on state. Therefore, the output voltage (V out) is low. The complementary inverter exhibited an excellent performance.

3. Conclusions

We reported two types of integrated circuits based on pentacene SITs and hybrid complementary inverters employing n-channel ZnO TFT and pentacene TFT for the first time. The inverters using pentacene SITs operated as low as a few voltages and have excellent transfer characteristics. These organic SIT inverters and hybrid complementary inverters are expected as key elements for flexible sheet displays.

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References

[1] K. Kudo, D. X. Wang, M. Iizuka, S. Kuniyoshi and K. Tanaka: Thin Solid Films **331** (1998) 51.

[2] Y. Watanabe, H. Iechi and K. Kudo: Jpn. J. Appl. Phys. **45, 4B** (2006) 3698.

[3] H. Klark, D. J.Gundlach and T. N. Jackson: IEEE Electron Device Lett.**20** (1999) 289.

[4] Y. Inoue, Y. Sakamato, T. Suzuki, M. Kobayashi, Y. Gao and S. Tokito: Jpn. J. Appl. Phys. **44** (2005) 3663.

[5] A. Dodabalapur, J. Baumbach, K. Baldwin, and H.E.Katz: Appl. Phys. Lett. **68** (1996) 2246.

[6] A. Dodabalapur, J. Laquindanum H.E.Katz, and Z.Bao: Appl. Phys. Lett. **69** (1996) 4227.