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3D System Integration: Enabling Technologies and Applications

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1. Introduction

For decades, huge efforts have been made to miniaturize microelectronic systems. In addition to chip scale packages (CSPs) and multichip modules (MCMs) that are commonly used now in a great variety of products, in the last few years 3D integration by package stacking and die stacking has come into high volume production.

Now the ITRS roadmap predicts an increasing demand for systems-on-a-chip (SoC) [1]. SoC fabrication is based on embedding multiple technologies, but there are serious disadvantages. The chip partition with the highest complexity drives the process technology, leading to a "cost explosion" of the overall system. In contrast, suitable 3D integration technologies enable the combination of different optimized base technologies (i.e. processors, SRAM, DRAM, analog, passives) with the potential of low cost fabrication through high yield and smaller IC footprints.

At the same time, the performance of microelectronic systems is more and more limited by the board-level wiring between the subsystems, causing a critical performance bottleneck. 3D integration is an emerging solution to this "wiring crisis," because it allows minimal interconnection lengths and the elimination of speed-limiting inter-chip interconnects.

The ITRS roadmap also shows an on-chip wiring crisis caused by signal propagation delay (RC delay). While copper has been integrated successfully into IC fabrication, the integration of low-k (<2.8) dielectrics has created reliability and yield problems, leading to significant implementation delays. The possible replacement of a large number of long interconnects by very short vertical interconnects due to 3D integration enables further shrinking according to Moore´s law without interconnect-limited performance.

2. Enabling Technologies for 3D System Integration

The large spectrum of 3D integration concepts can be classified in different ways, for instance chip-on-chip vs. wafer-to-wafer technologies, etc. Regarding the performance of the enabling technologies three main categories can be reasonably chosen:

- Stacking of Packages,
- Die Stacking and
- Vertical System Integration

Die Stacking with wire bonding for inter-chip interconnects is in production for several years by a number of companies. So-called "Chip-in-Polymer" technologies have been developed by e.g. IMEC, Fujitsu and Fraunhofer IZM. In these approaches thinned dies are stacked, embedded, and interconnected in a polymer layer with a modified multilayer thin film wiring [2].

A low cost die stacking approach was developed by Infineon in cooperation with Fraunhofer IZM [3]. The face-to-face stacking technology "SOLID" is based on solid-liquid inter-diffusion of thin electroplated and structured Cu/Sn layers, realizing both the mechanical bond and the electrical connections between the two dies.

Vertical System Integration (VSI) is characterized by very high density vertical inter-chip wiring with freely positioned through-Si vias. Requirements for VSI are a precise thinning technology including a cost-efficient handling concept, reliable formation of inter-chip vias, and a suitable bonding process. There are three main bonding schemes used for the fabrication of 3-D ICs: Oxide-oxide bonding, direct metal bonding, and adhesive bonding.

Fraunhofer IZM´s chip-to-wafer 3D technology – the so-called ICV-SLID process – is described in detail in [4]. Both the mechanical and the electrical connections between the chips are realized by solid-liquid-interdiffusion (SLID) of thin electroplated Cu/Sn layers. The thinned chips with tungsten- or copper-filled inter-chip vias (ICV) are connected to the bottom device wafer by the SLID system (Cu, Cu_3Sn ε-phase, Cu). The fully modular ICV-SLID concept allows the formation of multiple device stacks (see Fig.1).

3. Applications of 3D System Integration

In general the motivations for the introduction of 3D integration technologies into fabrication of microelectronic systems are

1. Packaging: Reduction of system volume, weight and footprint
2. Performance: Improvement of integration density and reduction of interconnect length resulting in improved transmission speed and reduced power consumption
3. Fabrication: Reduction of fabrication cost for mixed technologies products

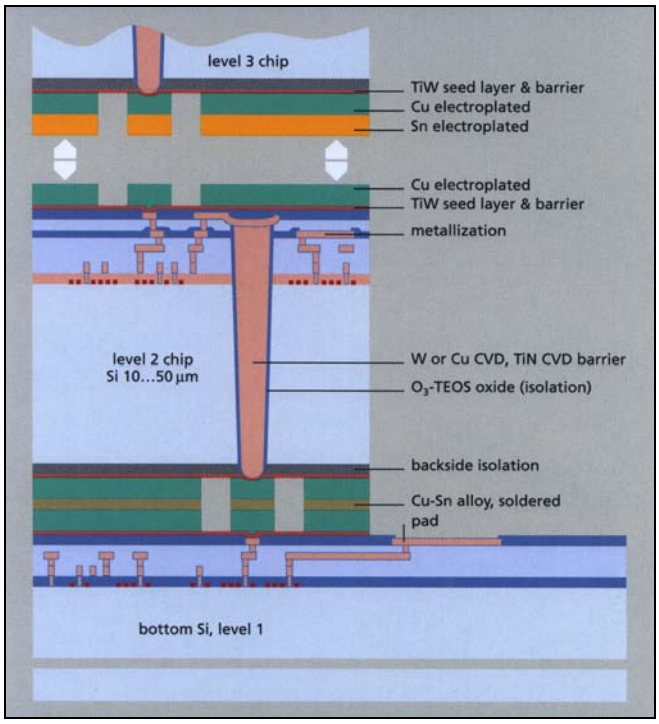

Fig. 1 Vertical System Integration by ICV-SLID technology: Schematic for the formation of multiple 3D-integrated device stacks (Cu-Sn-Cu eutectic bonding)

The potential for low cost fabrication is the key for applications of 3D integration. In competition to monolithic integrated SoCs, IC stacks (e. g. controller and memory layers) fabricated with optimized 3D integration technologies will show reduced production cost for e. g. automotive applications.

The introduction of 3D image processors and 3D CPUs will be mainly driven by the performance enhancement as emerging solutions to the on-chip "wiring crisis" caused by signal propagation delay. Suitable 3D integration technologies will be used to overcome the performance bottleneck caused by the predicted fundamental obstacles in backend-of-line.

Furthermore new multi-functional micro-electronic systems can be realized by 3D system integration: Ultra small smart systems for applications like e. g. distributed wireless sensor networks. The basic concept of a corresponding micro-system with different functions as sensors, microcontroller, wireless interface, memory, micropower source and power manager is shown in Fig. 2. For future applications, such systems for ambient intelligence will be highly miniaturized, so-called "electronic cubes" (e-CUBES®) with dimensions of 1 mm. 3D integration technologies have to be applied because of their relevant benefits: Extreme system volume reduction, reduction of power consumption (for lifetime enhancement), reliability improvement and low cost fabrication for meeting mass market requirements. In order to achieve cost effective solutions for a highly miniaturized e-CUBES® system, wafer-level 3D technologies will be used. Wafer yield and chip area issues speak against wafer stacking concepts for a mixed technologies product. In consequence chip-to-wafer technologies, mainly based on wafer-level processes utilizing known good dice only, have to be developed and optimized in order to meet the different requirements for integration of microelectronic devices, sensors and sub-modules as RF radio and power supply & management.

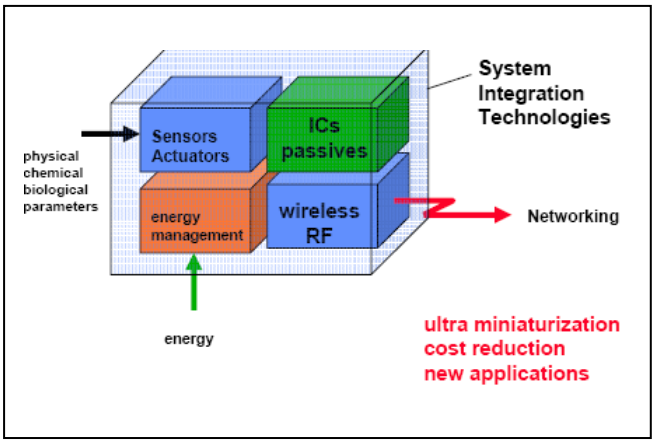

Fig. 2 Ultra small smart systems: Potential application of 3D system integration technologies for extreme miniaturization and low cost fabrication (e. g. wireless sensor networks)

Acknowledgements

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