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The Reliability Characteristics of Wafer-Level Chip-Scale Package under Various Current Stressing

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I. Introduction:

Improvements in semiconductor reliability are continuously being so far, they have been achieved. Recently, the wafer level chip scale package (WL-CSP) was developed under the demand of small outline, lightweight, high I/O density, and good electrical performance for mobile consumer electronic devices such as cellular phones, pagers, and PDA's. In general, wafer level chip scale packages, first designed to eliminate the need for encapsulation, to be SMT-processes compatible, and to have good handling properties, etc., face some reliability problems.

The trend in VLSI technology has resulted in not only narrower interconnection lines but also smaller contacts. [1] This has aggravated the electromigration-induced failure problems which were especially critical in the field of wafer level chip scale package. To achieve design in reliability, one must be able to determinate the maximum current density guideline in the conductors and at the contacts and have the ability to efficiently analyze and correct potential electromigration failures during the circuit design phase [2-3].

In this paper, a modeling of electromigration MTTF (mean time to failure) as a function of various dc current densities was well established. Besides, the failure mode analysis was also examined by using SEM.

II. Experimental:

In this paper, The WL-CSP test vehicle was constructed by surface mounting a 6.35 mm x 6.8 mm daisy-chained chip onto a daisy-chained test board through 98 ea I/O with material of 95.5 Sn-4Ag-0.5Cu solder joints, as shown in Fig. 1. The surface finish of board pads was electro less plated Ni/Au. The under bump metallurgy (UBM) on the chip side was a stack of sputtered thin films of 4 kÅ Al / 3.25 kÅ Ni (V) / 8 kÅ Cu while the trace was also a stack of 2 kÅ Ti / 15 kÅ Al / 2 kÅ Ti. The pitch between adjacent solder joints was 500 um. The UBM opening was 280 um in diameter.

The equipment set up for this measurement consists of a regulated power supply, an electronic load, a heat oven, and a digital multi-meter. The heat oven is used to perform thermal aging and controlled at temperature at 125 ^{0}C. The experimental detailed parameters were listed as Table-1.

III. Results:

Electromigration is the moment of metal atoms in the direction of current flow. The model can be described as:

$$MTTF = AW^{p}L^{q}J^{-n}\exp(E_a / kT)$$

Where J is current sensity, Ea is activation energy, W is the width of metal, and L is the length. It is caused by the transfer of momentum from the passing electrons to atoms in the lattice. Fig. 2 and Fig. 3 were the results of resistance under current stressing conditions at J=0.5 and 0.7 Amp, respectively, under a fixed ambient temperature of 125 ^{o}C. Simultaneously, the MTTF was defined as the duration of stressing time before metal line resistance tempestuously increasing. This power-law model is a simplified version of the phenomenal Black's equation, which is usually employed in characterizing the electromigration reliability of conductors and shown in Fig. 4. Fig. 5 had represented the architecture of cross section of chip scale package in this experimental. In this figure, the failure sites were marked with black dotted line.

It is important to examine the failure mode at the samples after current stressed by various current densities. Fig 6 shows that a consummation reaction of Cu was happened at the corner of solder bump. This reaction was also occurred at other current densities of 0.5, 0.6, 0.7, 0.8, and 0.9 Amp. Fig. 7 shows that the stressing current will cause the runner become thinner. This phenomenon will become more critical in higher current density. Besides, there is another failure site at near the trace. A crack was occurred after current stressing, which was shown in fig. 8.

Conclusions:

In this paper, the reliability of WLCSP under accelerated current stressing conditions of 0.5 A, 0.6 A, 0.7 A, 0.8A, and 0.9 A at a fixed ambient temperature of 125 ^{o}C was investigated.

The cross-sectional examinations of the solder joints were taken by SEM. There are three type of failure mode were presented: (1) the solder bump occurs copper consummation reactions, (2) the runner become thinning, and (3) the trace was occurring crack.

References:

[1]. Lee Teck Kheng, Teo Yong Chua and Lim Thiam Beng, IEEE /CPMT Electronics Packaging Technology Conference proceeding, (1998), pp. 274-278.

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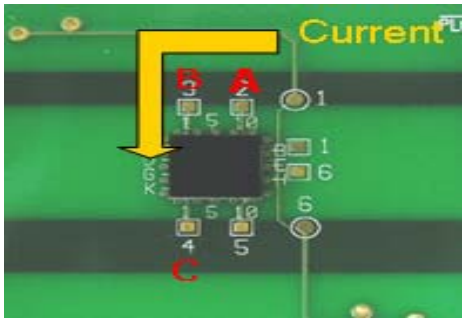

Fig. 1 The top view picture of wafer level chip scale package (WL-CSP) which were after Surface Mount Technology (SMT) process.

Table- I The experimental used conditions.

Package Type	WLCSP
Package Dimensions	6.35x6.8
Passivation Type	Polymide
Die Size	6.35x6.8
UBM	4KA Al / 3.25KA NiV / 8KA Cu
UBM opening	280 um
Runner	2KA Ti / 15KA Al / 2KA Ti
Bump Composition	Sn/Ag4.0/Cu0.5
No. of bump	98
Bump pitch	0.5mm
Ball Size	0.3mm
Ball pitch	0.5mm
Surface finishing	Au/Ni
Board thickness	0.8 mm
Pad	NSMD

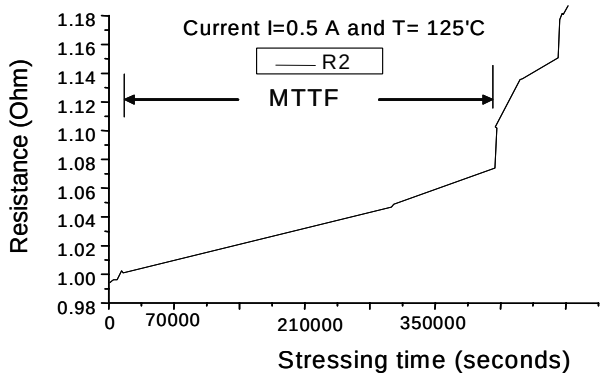

Fig. 2 The results of resistance under current stressing conditions at J=0.5 Amp. and a fixed ambient temperature of 125 °C.

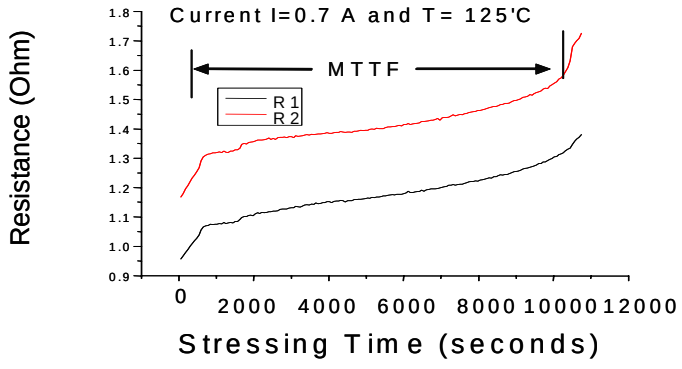

Fig. 3 The results of resistance under current stressing conditions at J=0.7 Amp. and a fixed ambient temperature of 125 °C.

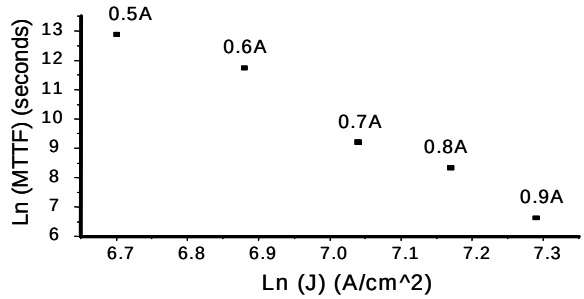

Fig. 4. Correlation between N_f and J at a fixed ambient temperature of 125 °C

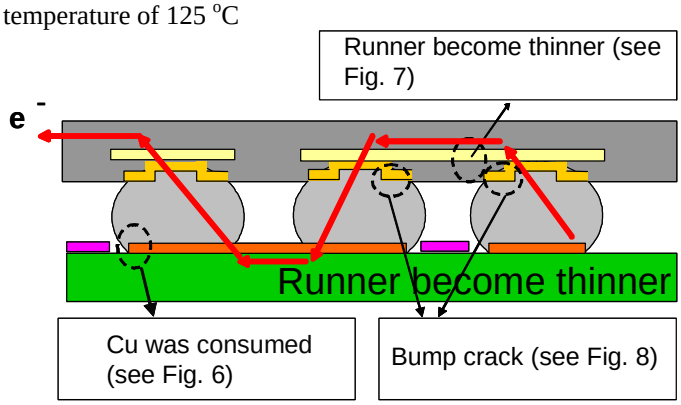

Fig. 5. A diagram was shown for failed site.

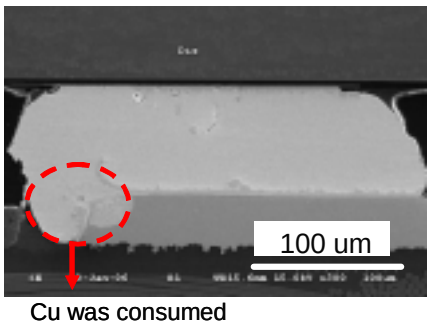

Fig. 6 The failure mode analyzed by SEM at solder bump.

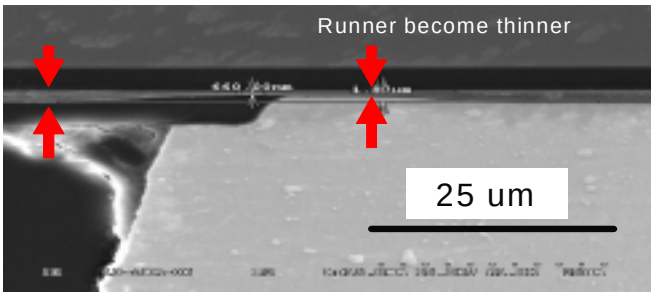

Fig. 7 The failure mode analyzed by SEM at runner corner.

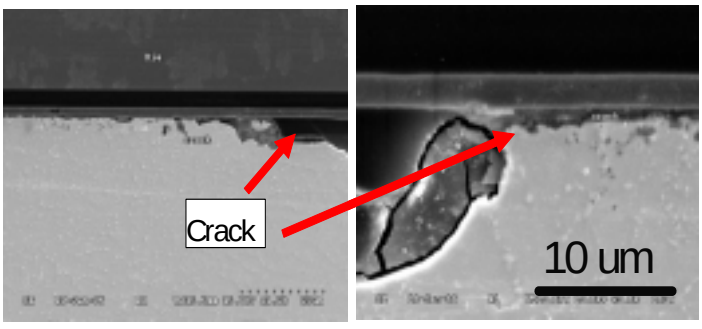

Fig. 8 The failure mode analyzed by SEM between UBM and solder bump.